

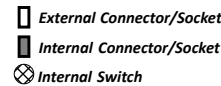
NM-D271


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- 4.CPU (2/16): DDR (1/2)
- 5.CPU (3/16): DDR (2/2)
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- 7.CPU (5/16): ESPI/SPI/SMBUS/C-LINK
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- 11.CPU (9/16): CSI-2/EMMC/CNVI
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- 22.BLANK
- 23.BLANK
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- 28.BLANK
- 29.BLANK
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- 66.WLAN
- 67.M.2 SOCKET
- 68.DDI DEMULTIPLEXER
- 69.USB TYPE-A CONNECTOR
- 70.USB TYPE-A CONN

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75.LAN_B CONNECTOR	10
76.MEDIA CARD CONTROLLER	10
77.MEDIA CONNECTOR	10
78.AUDIO ALC3287	10
79.AUDIO CONNECTOR	10
80.AUDIO JACK SENSE	10
81.AUDIO EXT MIC I/F	10
82.AUDIO SPEAKER	10
83.AUDIO BEEP	10
84.AUDIO DEBUG	10
85.EC_NPCE68APA0DX(1/2)	10
86.EC_NPCE68APA0DX(2/2)	10
87.BLANK	10
88.KEYBOARD/TRACK POINT	10
89.TOUCH PAD/NFC/FPR	10
90.FAN CONNECTOR	10
91.APS G-SENSOR	10
92.THERMAL SENSOR	10
93.SMBUS SWITCH	10
94.BLANK	10
95.BLANK	10
96.BLANK	10
97.SATA Re-driver	10
98.DISCRETE TPM 2.0	10
99.SCREW HOLES	10
100.DC-IN	10
101.BATTERY INPUT	10
102.BATTERY CHARGER(BQ25700A)	10
103.DC/DC VCC5M (LV6228C)	10
104.DC/DC +5VTPC(LV6228C)	10
105.DC/DC VCC3M (SYX198B)	10

106.DC/DC VCC1R2A(SY8310RAC)
107.DC/DC VCC2R5A(RT8068A)
108.DC/DC IMVP8(RT3613EE)
109.DC/DC VCCCPUCORE (RT9610CGQ)
110.DC/DC VCCPCHCORE (RT6543)
111.BLANK
112.DC/DC Decoupling Cap
113.BLANK
114.BLANK
115.BLANK
116.DC/DC VCC1R8_SUS(RT8068A)
117.DC/DC VCCGFXCORE_D(NCP81278)
118.DC/DC VCC1R2VIDEO(MP2941)
119.DC/DC VCC1R8VIDEO_AON(BD9B304)
120.DC/DC VCC1R0VIDEO(BD9B304)
121.BLANK
122.BLANK
123.LOADSW VCCST&VCCSTG
124.LOAD SW PCH SUS
125.LOAD SW SSD/CR
126.LOAD SW LAN
127.LOAD SW B
128.LOAD SW WLAN
129.PLM BOM

Project Code: HL4A0/HL5A0

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Issued Date	2018/01/12	Deciphered Date		BLOCK DIAGRAM		
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DDR4 CHANNEL 0

DDR4 non interleaved Type

UCPU1B

2 OF 21

DDR4 AN3LP4

DDR4 AN3LP4

[13,16,51,52,55,56,59,84,85,86,88,102,103,104,105,106,110,116,118,119,120,123,124,125,126,127,128]

[5,14,15,33,34,35,36,106]

VCC1R2A

M_A_VREF_CA

VCC3M

VCC3M

M-A-DQ0

M-A-DQ1

M-A-DQ2

M-A-DQ3

M-A-DQ4

M-A-DQ5

M-A-DQ6

M-A-DQ7

TGLLAKE-U, BGA1449

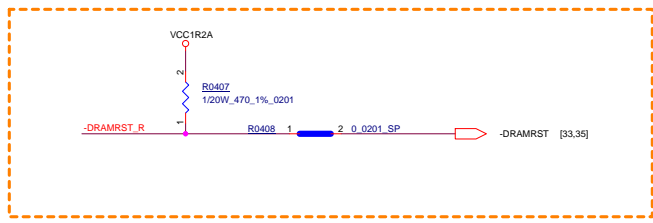
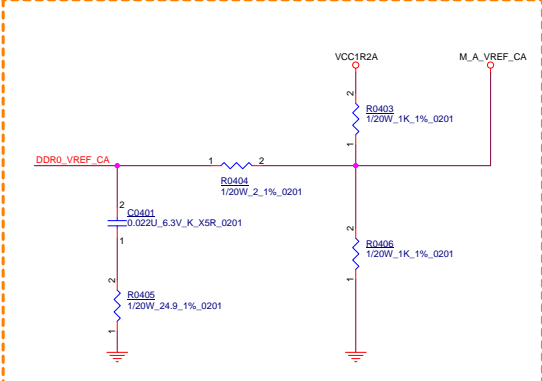
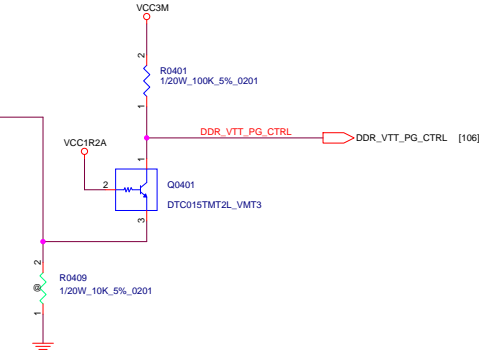


TABLE of (Q0401)		
Vendor	LCFC P/N	Description
ROHM	SB00000WCOJ	S TR DTC015TMT2L NPN VMT3
TOSHIBA	SB000010700	S TR RN1131MFV NPN VESM
ON	SB000013J00	S TR DTC115TM3T5G NPN SOT-723-



DDR4 CHANNEL 1

M-B-DQ0

M-B-DQ1

M-B-DQ2

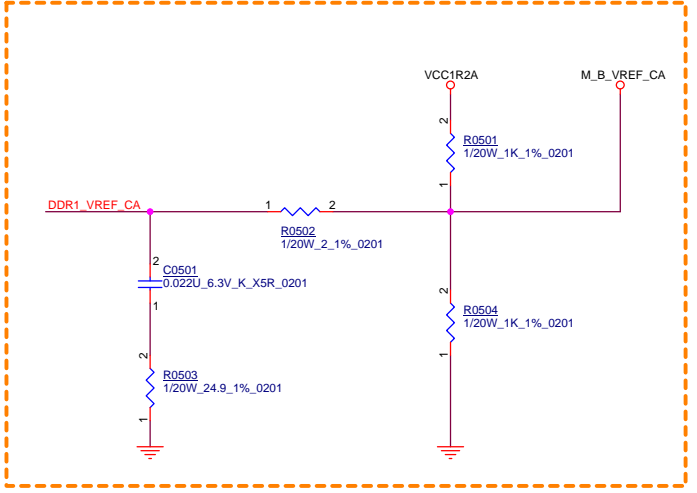
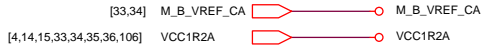
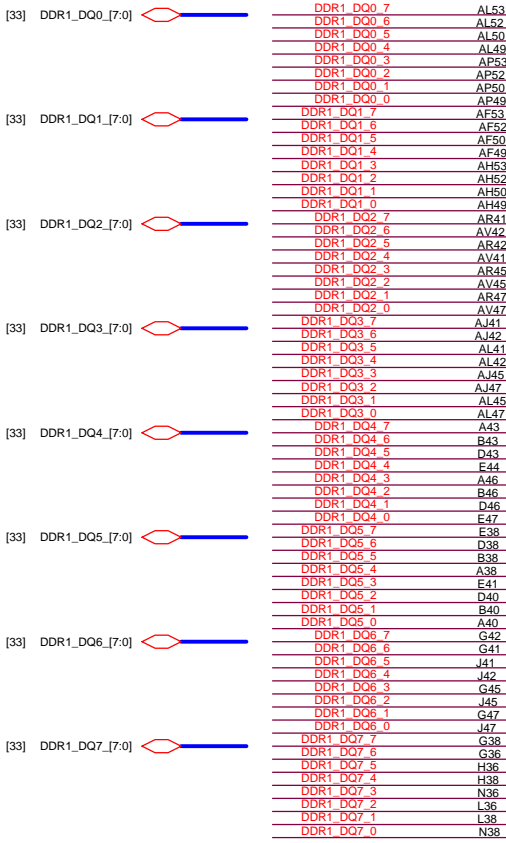
M-B-DQ3

M-B-DQ4

M-B-DQ5

M-B-DQ6

M-B-DQ7



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Issued Date	2015/09/01	Deciphered Date	2016/12/31
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Title				Rev 1.0
TGL(C)_DDR4 CH.B				
Size Custom	Document Number	HL4A0/HL5A0 NM-D271		
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TABLE : Functional Strap

DBG_PMODE (DFx Test Mode)	
HIGH	DFx Test Mode Disabled (default) *
LOW	DFx Test Mode Enabled

TABLE : Functional Strap

GPP_F7 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

GPP_F10 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration (Default)

[3,7,8,10,13,16,21,37,40,50,51,72,93,98,117,123,124]
[13,14,108,123]
[14,123]
[14]
VCC3_SUS
VCCST
VCCSTG
VCCSTG_TERM

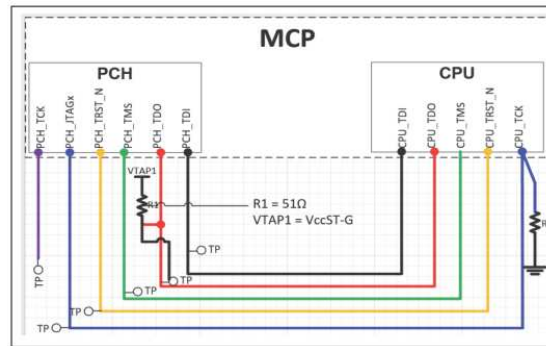
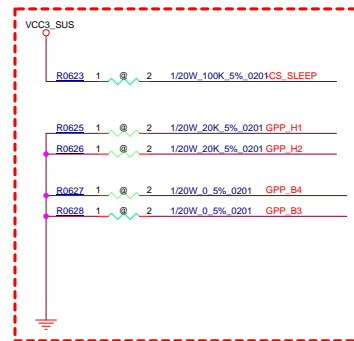
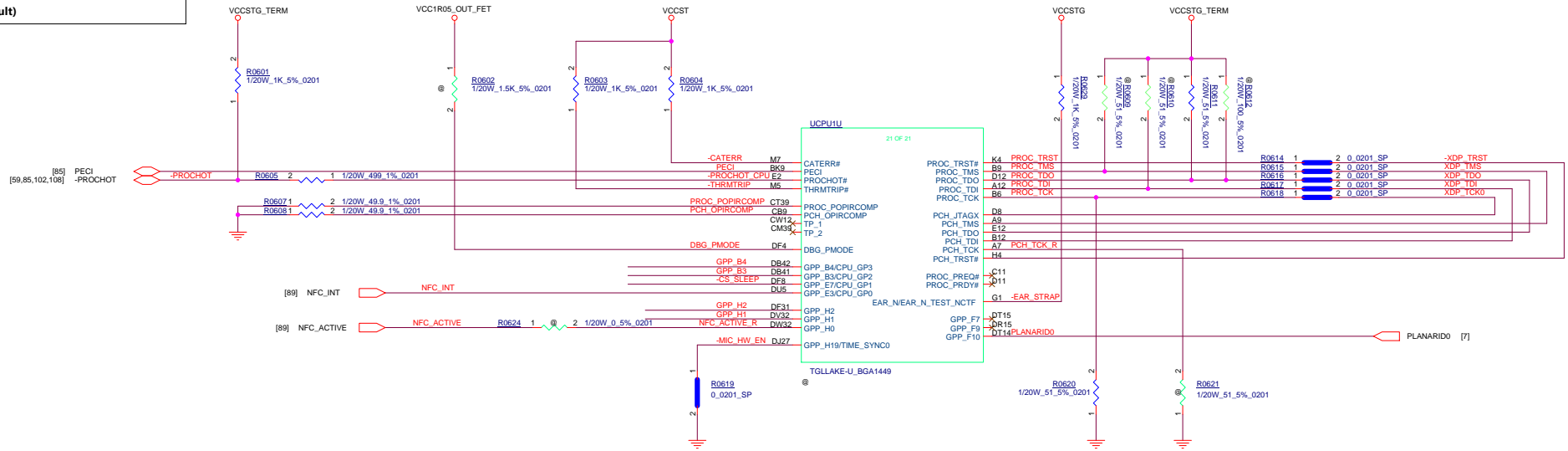


TABLE : Functional Strap		
SPI0_MOSI (Boot Halt)		
HIGH	Disabled	*
LOW	Enabled	

TABLE : Functional Strap		
SPI0_IO3 (AO Personality Strap)		
HIGH	Disabled	*
LOW	Enabled	

TABLE : Functional Strap		
SPI0_IO2 (Consent Strap)		
HIGH	Disabled	*
LOW	Enabled	

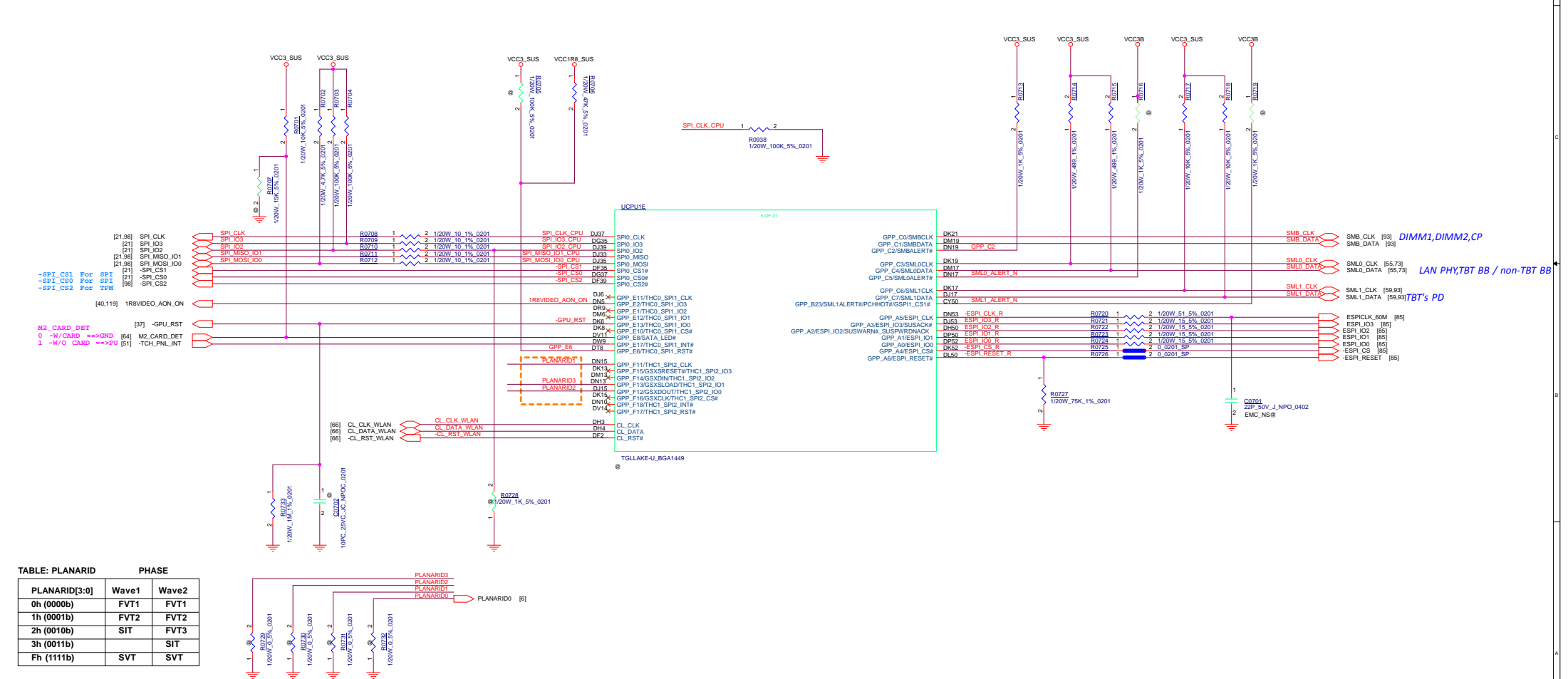
TABLE : Functional Strap		
GPP_E6 (JTAG ODT Disable)		
HIGH	JTAG ODT Enabled	*
LOW	JTAG ODT Disabled	

TABLE : Functional Strap		
GPP_C2/SMBALERT# (TLS Confidentiality)		
HIGH	Enable ME Crypto TLS with Confidentiality	*
LOW	Disable ME Crypto TLS (Default)	

TABLE : Functional Strap		
GPP_B23/SML1ALERT#/PCHHOT# (CPUNSSC Clock Frequency)		
HIGH	19.2MHz Clock (Derived from 38.4MHz Crystal)	
LOW	38.4MHz Clock (Direct from Crystal)	*

TABLE : Functional Strap	
GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration (Default)

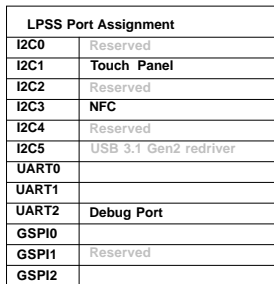
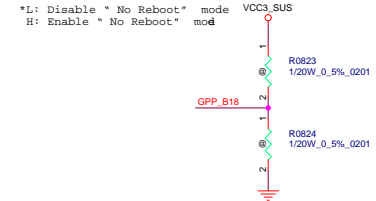
SPI0_MOSI	Reserved	Rising edge of RSMRST# External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST# External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST# External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default) *

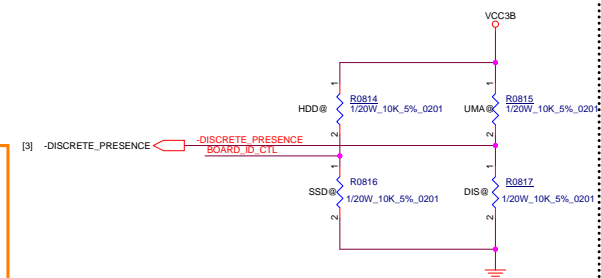
GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default) *

GPP_B18, Internal PD 2



Status	-DISCRETE- PRESENCE (GPP E18)
DIS	0 (R0817)
UMA	1 (R0815)

Status	BOARD_ID_CT (GPP_D14)
SSD	0 (R0816)
HDD	1 (R0814)




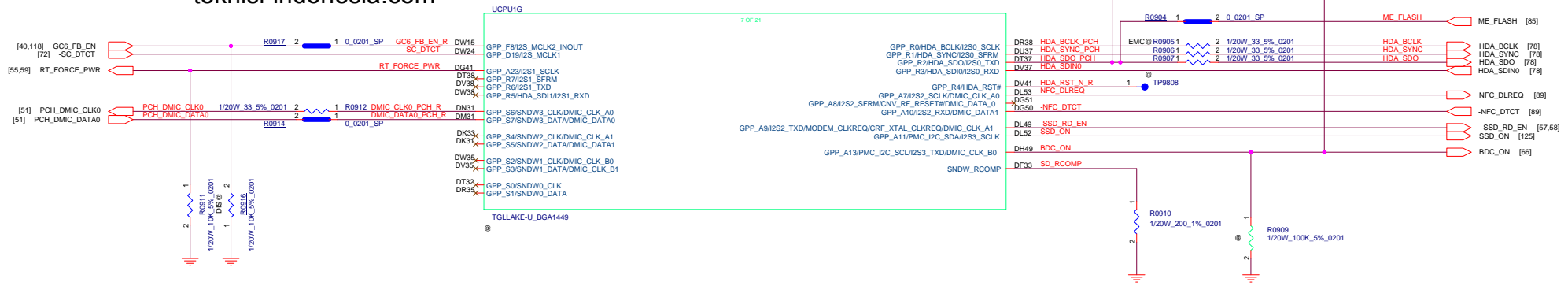
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Size C	Document Number HL4A0/HL5A0 NW-D271				
Date:		Tuesday, October 13, 2020		Sheet 8 of 130	

TABLE : Functional Strap

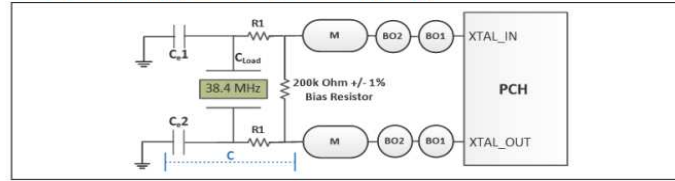
GPP_R2/HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

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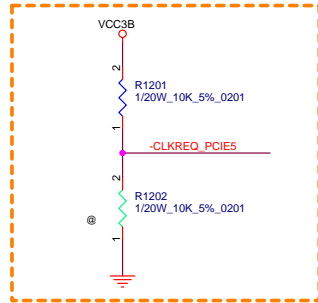
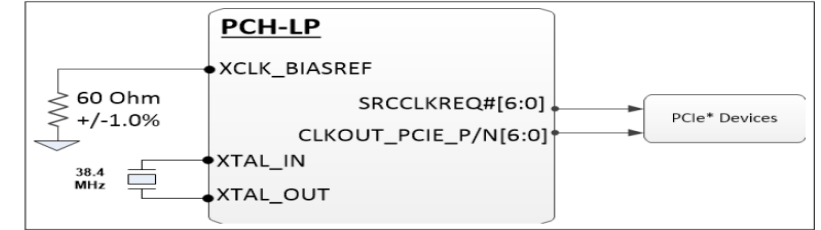
PCH-LP Platform XTAL Routing Guidelines

Figure 62. PCH-LP Platform Crystal XTAL_IN/OUT Topology



6.1.1 Interface Details

Figure 60. Clock Integration Distribution Diagram



PCIe CLK Table	
CLK 100M_P0	SSD
CLK 100M_P1	LAN
CLK 100M_P2	Media Card Reader
CLK 100M_P3	GPU
CLK 100M_P4	WWAN
CLK 100M_P5	Reserved
CLK 100M_P6	WLAN

CLKREQ Table	
CLKREQ0	SSD
CLKREQ1	LAN
CLKREQ2	Media Card Reader
CLKREQ3	GPU
CLKREQ4	WWAN
CLKREQ5	Reserved
CLKREQ6	WLAN

TABLE of Y1201		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00
Harmony	X2CL038400DA1H-HU	SJ10000XS00
KDS	7AF03840A04	SJ10000XG00

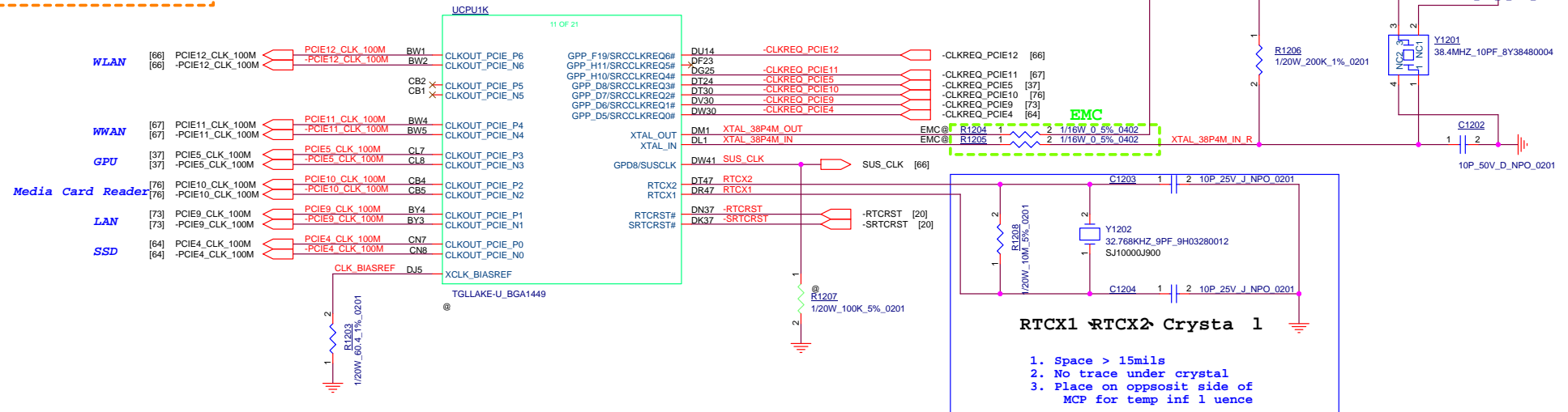

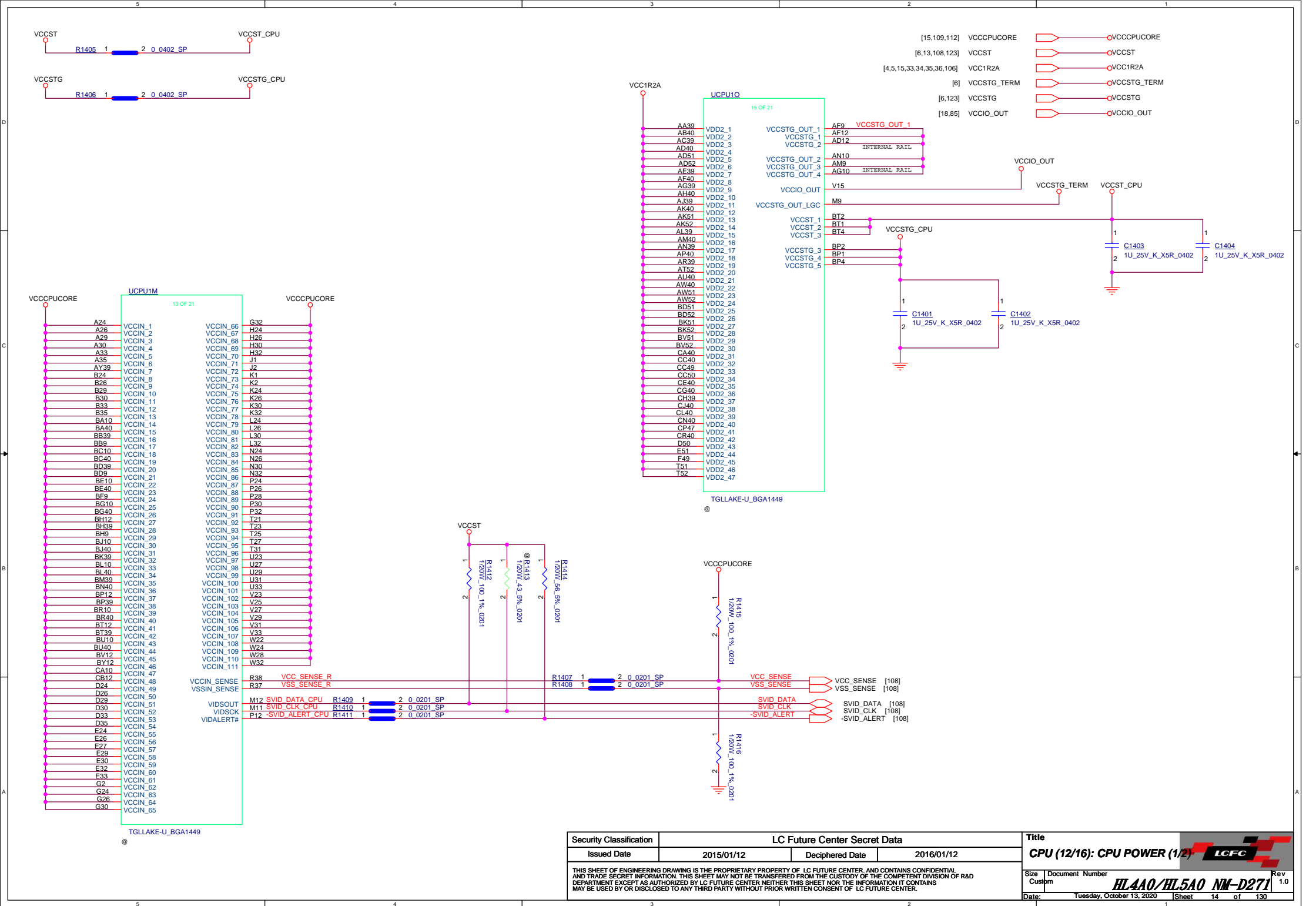


TABLE of XTAL (Y1202)		
Vendor	LCFC P/N	Description
TXC	SJ10000J900	S CRYSTAL 32.768KHZ 9PF 20PPM
KDS	SJ100069400	S CRYSTAL 32.768KHZ 9PF 1TJF09
SEIKO	SJ10000IX00	S CRYSTAL 32.768KHZ 9PF X1A000

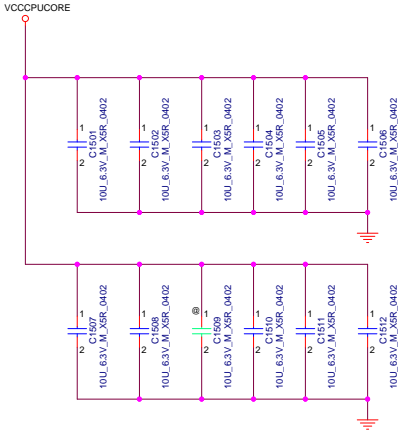
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					HL4A0/HL5A0 NM-D271 Rev 1.0
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VCCCPUCORE CAP IN PWR SHEET

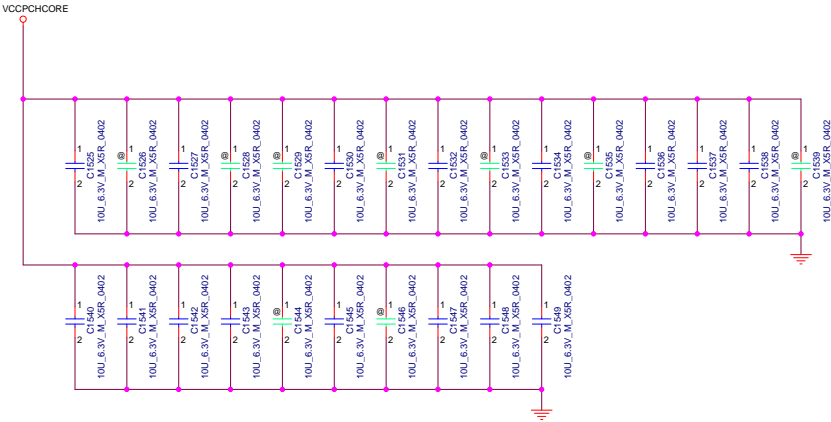
VCCCPUCORE	PDG	LCFC
330uF_B2 (CS)	2	HW: 0 / PWR: 1
22uF_B2 (CS)	8	HW: 0 / PWR: 2
10uF_0402 (CS)	12	HW: 12 / PWR: 0



CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN

VCCPCHCORE CAP IN PWR SHEET

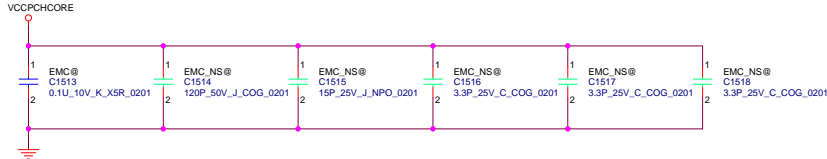
VCCPCHCORE	PDG	LCFC
330uF_B2 (CS)	1	HW: 0 / PWR: 0
220uF_B2 (CS)	1	HW: 0 / PWR: 1
47uF_0805 (CS)	3	HW: 0 / PWR: 3
22uF_0603 (CS)	12	HW: 0 / PWR: 12
10uF_0402 (CS)	15	HW: 15 / PWR: 0
10uF_0402 (SS)	10	HW: 10 / PWR: 0



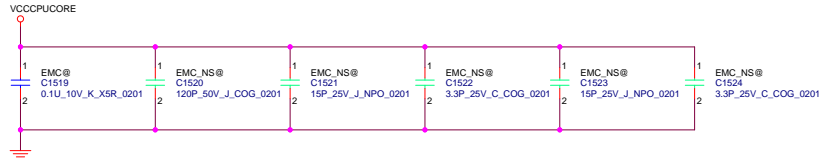
CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN_AUX

EMC

[16,110,112]	VCCPCHCORE	VCCPCHCORE
[14,109,112]	VCCCPUCORE	VCCCPUCORE
[4,5,14,33,34,35,36,106]	VCC1R2A	VCC1R2A



EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN_AUX

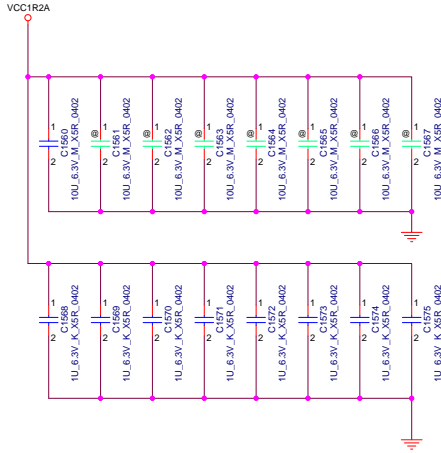


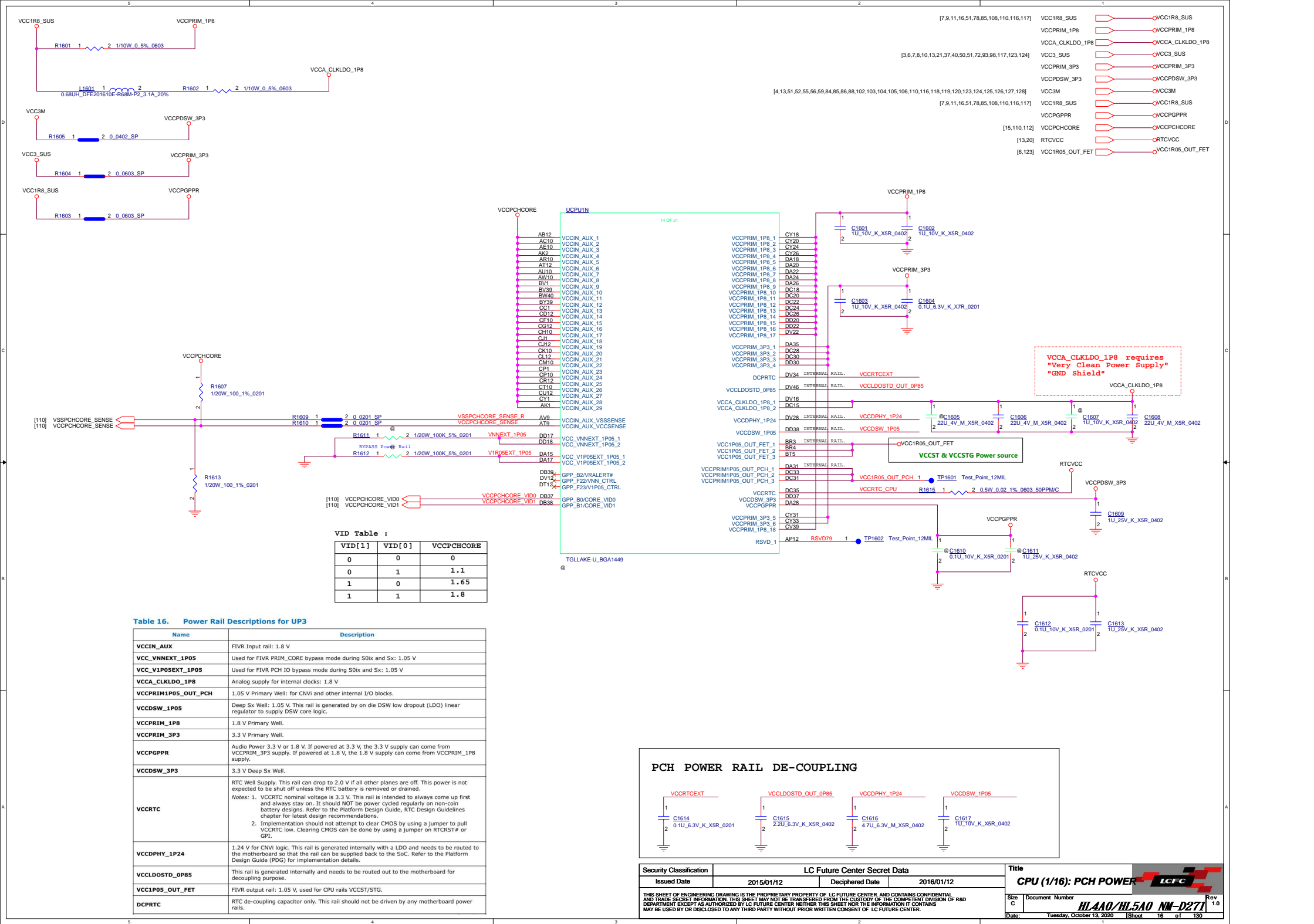
EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN

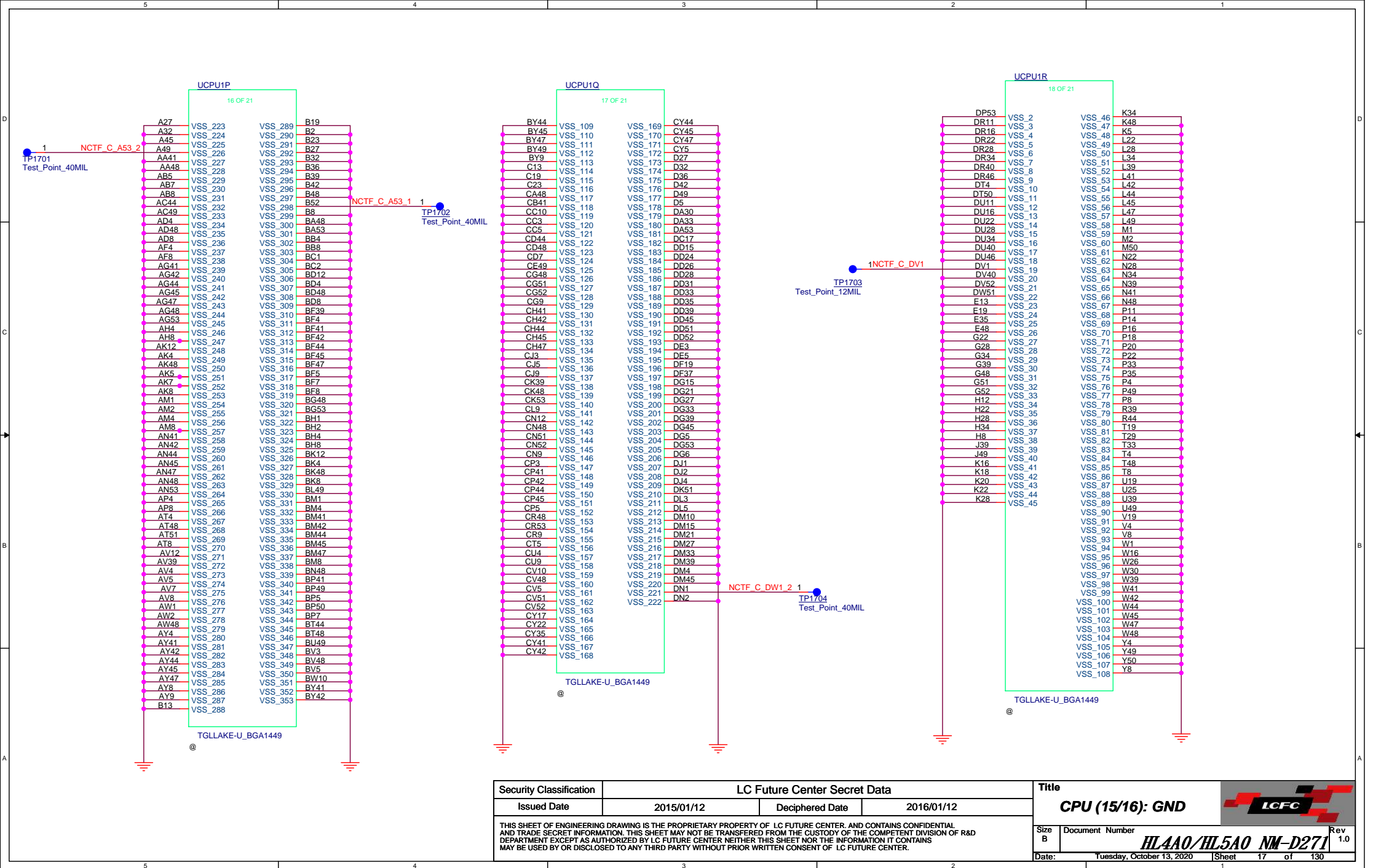
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VCC1R2A CAP

VCC1R2A_CPU	PDG Requirement	LCFC Design
47uF_0603 (CS)	2	HW: 0 / PWR: 0
22uF_0603 (CS)	0	HW: 0 / PWR: 6
10uF_0402 (SS)	8	HW: 8 / PWR: 0
1uF_0402 (CS)	8	HW: 8 / PWR: 0







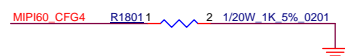
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Size B		Document Number		HL4A0/HL5A0 NM-D271	
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PROCESSOR CFG STRAPS

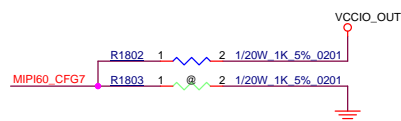
```
.....
eDP  Enable
```

```
CFG4      1:Disable
          .....
          * 0:Enable(Default)
```



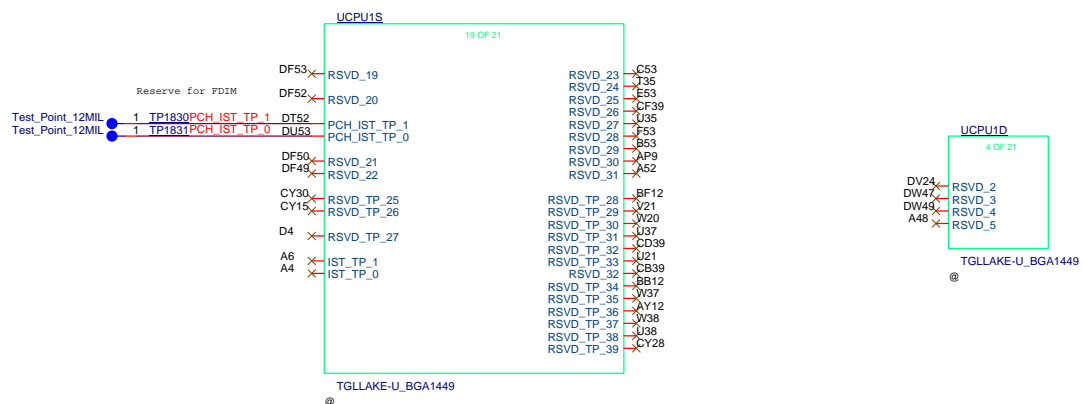
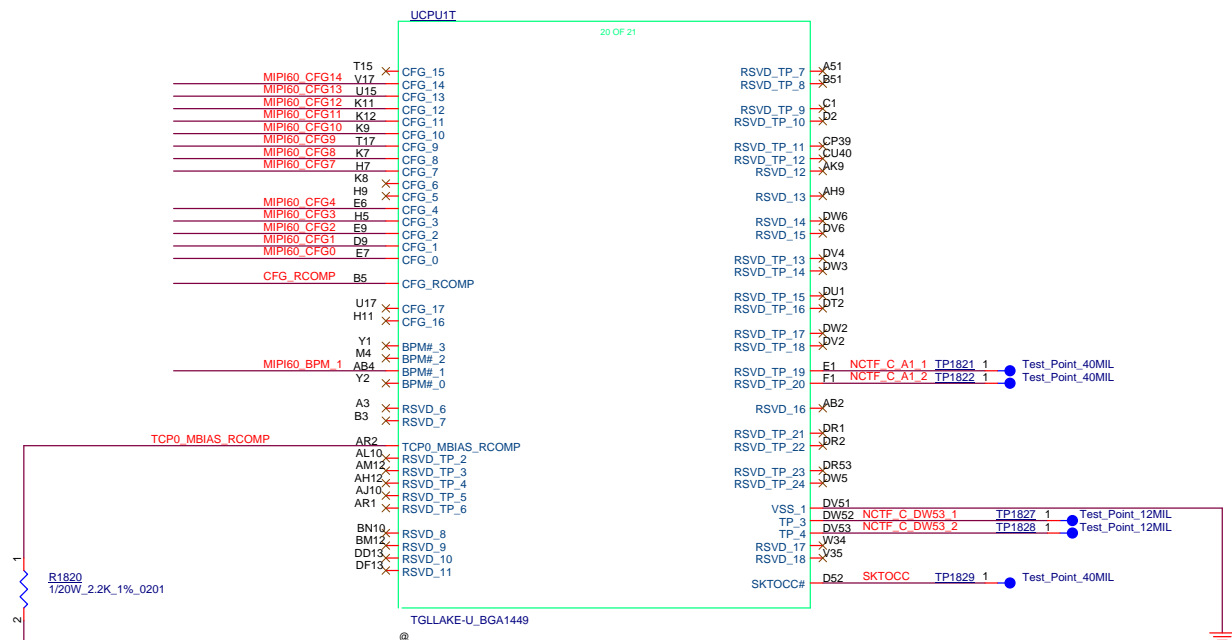
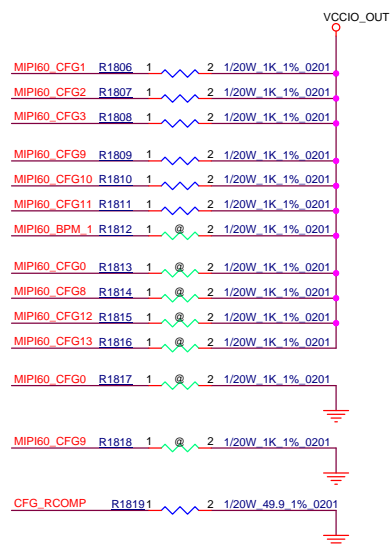
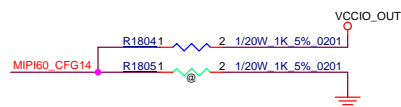
PEG Deferred Link Training


CFG7	* 1:Enabled 0:Disabled
------	---------------------------




PEG60 Lane Reversal

```
CFG14  *1:Normal (Default)
        0:Resersal
```



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RTCVCC ○ — □ RTCVCC [13,16]

RTC CONN.

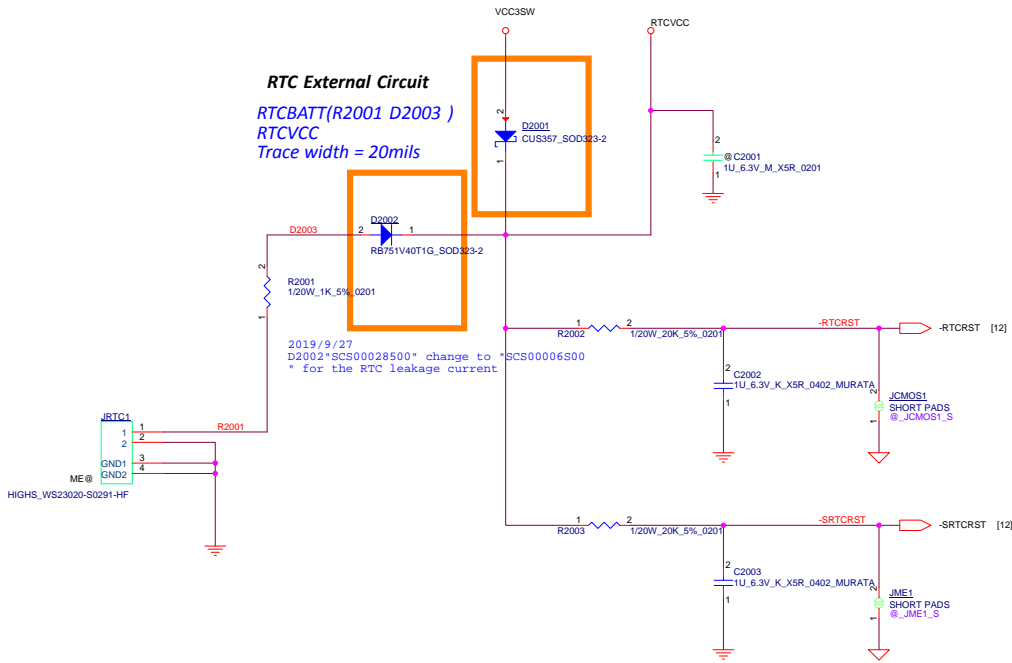
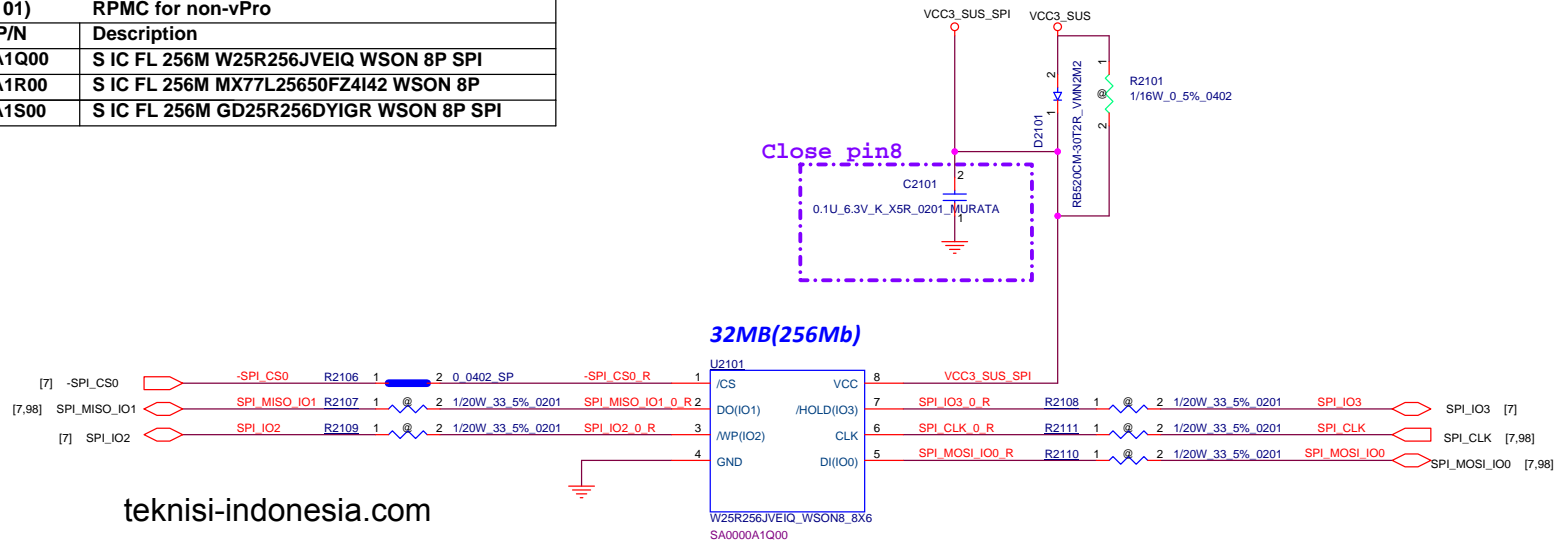


TABLE of SPI ROM (U2101)		RPMC for non-vPro
Vendor	LCFC P/N	Description
Winbond	SA0000A1Q00	S IC FL 256M W25R256JVEIQ WSON 8P SPI
MXIC	SA0000A1R00	S IC FL 256M MX77L25650FZ4I42 WSON 8P
GD	SA0000A1S00	S IC FL 256M GD25R256DYIGR WSON 8P SPI

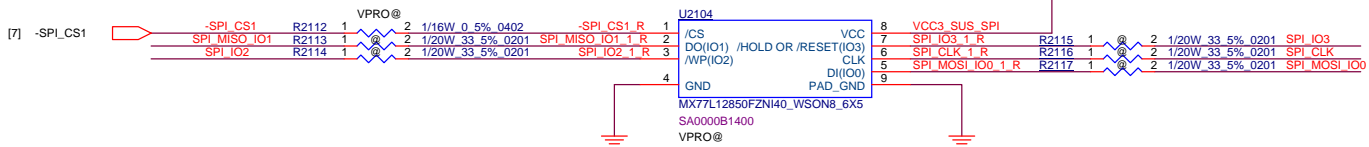
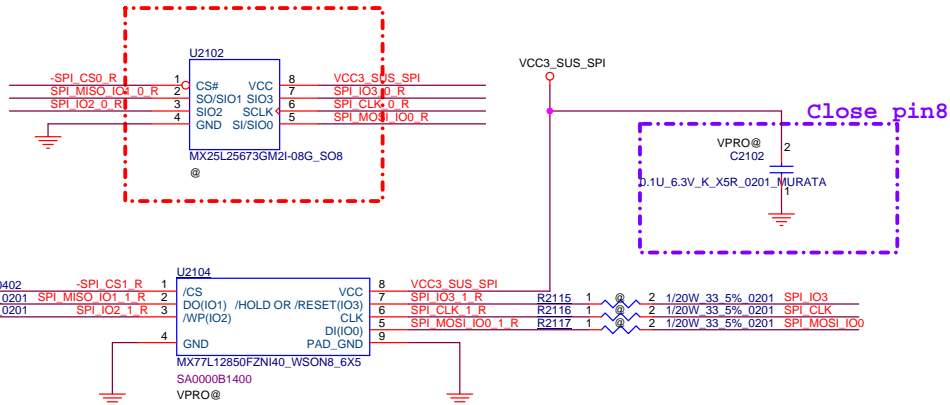


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TABLE of SPI ROM (U2102)		non RPMC for vPro
Vendor	LCFC P/N	Description
MXIC	SA00008J400	S IC FL 256M MX25L25673GM2I-08G SOP 8P
Winbond	SA00008WZ00	S IC FL 256M W25Q256JVEIQ WSON 8P SPI
GD	SA00009R800	S IC FL 256M GD25B256DYIGR WSON 8P SPI

32MB (256Mb) 200MIL SOIC8
MACRONIX MX25L25673GM2I-08G
MACRONIX MX25L25673GM2I-10G

32MB (256Mb) 8x6mm WSON8 (Optional)
WINBOND W25Q256JVEIQ



vPro TABLE (VPRO@)	
LCFC P/N	SD00000LHYT
Description	1/20W_33_5%_0201
Location	R2107,R2108,R2109,R2110,R2111 R2113,R2114,R2115,R2116,R2117


Non-vPro TABLE (NVPRO@)	
LCFC P/N	SD00000LIYT
Description	1/20W_56_5%_0201
Location	R2107,R2108,R2109,R2110,R2111

TABLE of U2104		
Vendor	P/N	LCFC P/N
MXIC	MX77L12850FZNI40 WSON	SA0000B1400
Winbond	W25R128JVPIQ WSON	SA0000B2Z00
GD	GD25R127DWIG WSON	SA0000B3C00


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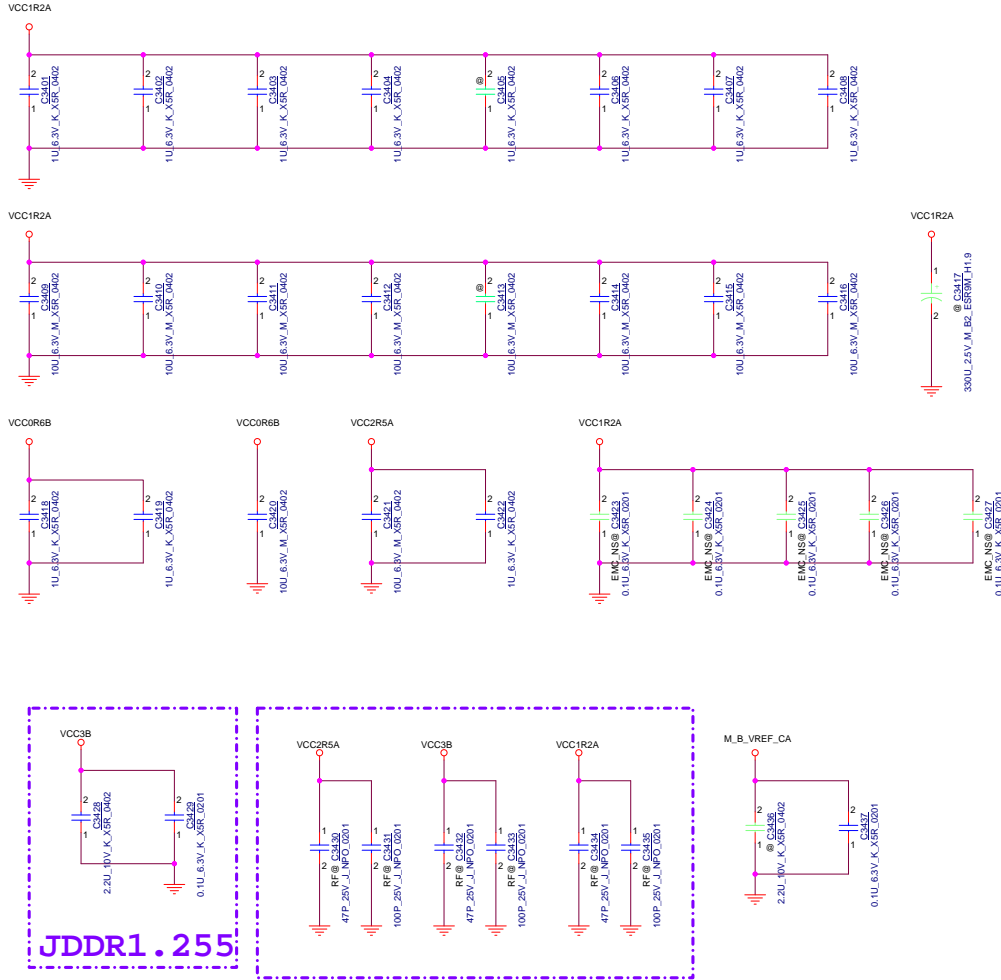
VCC1R2A	PDG	LCFC
1uF_0402	8	HW:8/PWR:0
10uF_0603	8	HW:8/PWR:0
330uF_B2	1	HW:0/PWR:0

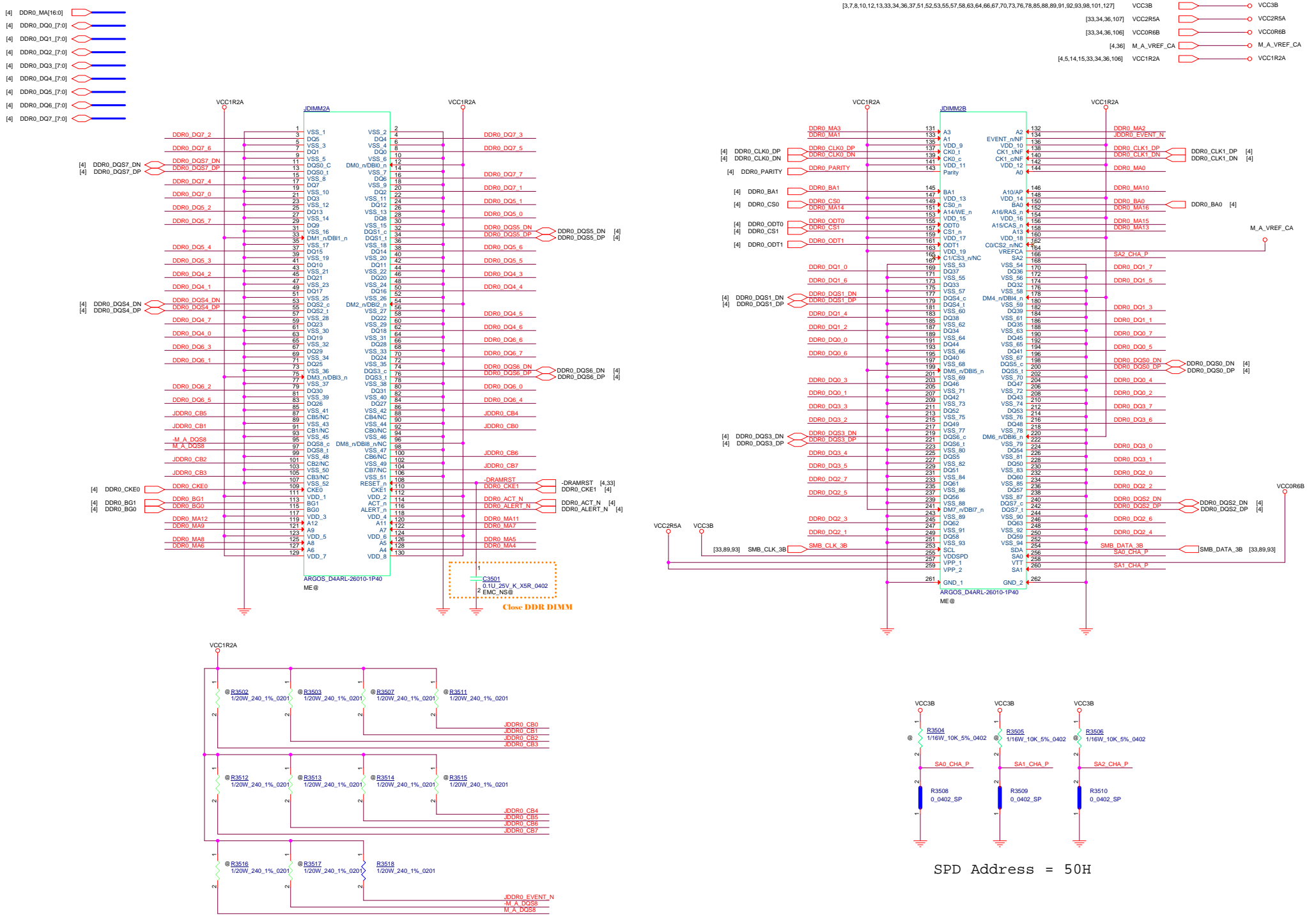
JDDR1.255	PDG	LCFC
0.1uF_0402	1	HW:1/PWR:0
2.2uF_0402	1	HW:1/PWR:0

VCC0R6B	PDG	LCFC
1uF_0402	2	HW:2/PWR:0
10uF_0603	1	HW:1/PWR:0

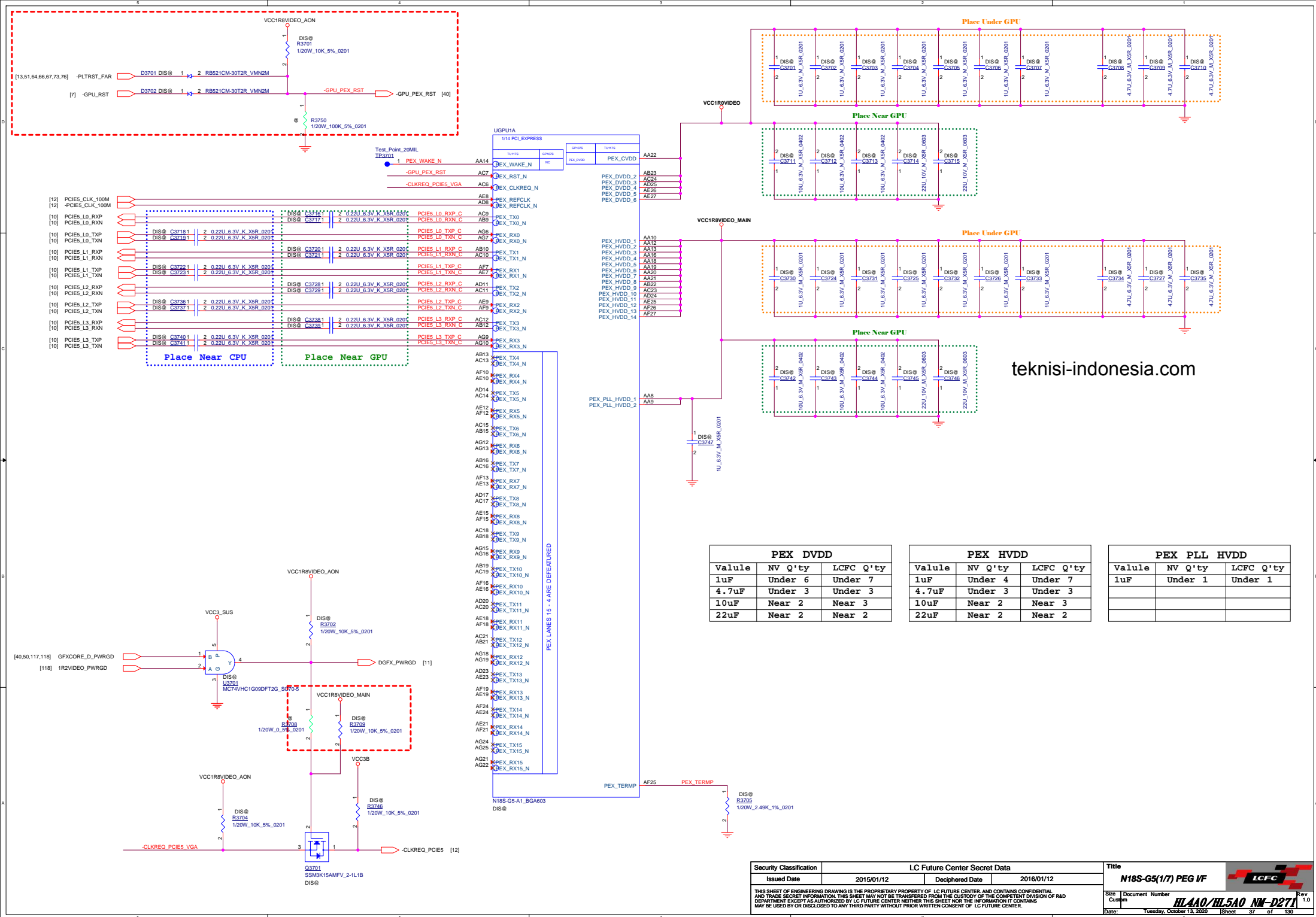
VCC2R5A	PDG	LCFC
1uF_0402	1	HW:1/PWR:0
10uF_0603	1	HW:1/PWR:0

[33,35,36,106]	VCC0R6B		VCC0R6B
[4,5,14,15,33,35,36,106]	VCC1R2A		VCC1R2A
[33,35,36,107]	VCC2R5A		VCC2R5A
[3,7,8,10,12,13,33,35,36,37,51,52,53,55,57,58,63,64,66,67,70,73,76,78,85,88,89,91,92,93,98,101,127]	VCC3B		VCC3B
[5,33]	M_B_VREF_CA		M_B_VREF_CA



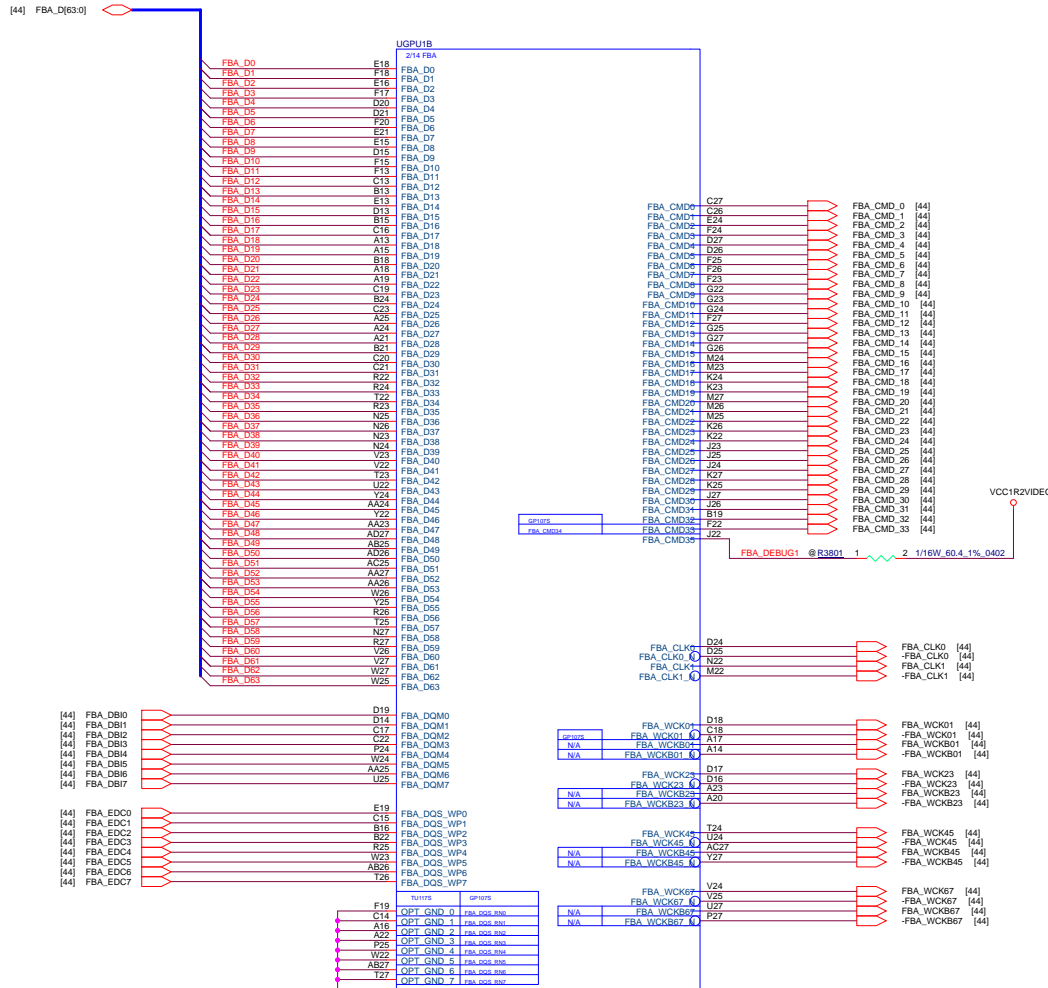


SPD Address = 50H



N18S-G5 **Package : GB2E-64** **NV Symbol : TU117S**

	0..31		32..63		Pin
	DRAM1		DRAM2		Loading
	CHA	CHB	CHA	CHB	
	Bytes 0,1		Bytes 4,5		Bytes 6,7 x16 mode
CMD0	CA0_A				1
CMD9	CA1_A				1
CMD8	CA2_A				1
CMD32	CA3_A				1
CMD4		CA0_B			1
CMD12		CA1_B			1
CMD5		CA2_B			1
CMD13		CA3_B			1
CMD7	CA4_A	CA4_B			2
CMD11	CA5_A	CA5_B			2
CMD15	CA6_A	CA6_B			2
CMD14	CA7_A	CA7_B			2
CMD3	CA8_A	CA8_B			2
CMD1	CA9_A	CA9_B			2
CMD6	CAB1_A	CAB1_B			2
CMD10	CKE_A	CKE_B			2
CMD2	RST*				1
CMD20			CA0_A		1
CMD28			CA1_A		1
CMD21			CA2_A		1
CMD29			CA3_A		1
CMD16				CA0_B	1
CMD25				CA1_B	1
CMD24				CA2_B	1
CMD33				CA3_B	1
CMD23			CA4_A	CA4_B	2
CMD27			CA5_A	CA5_B	2
CMD30			CA6_A	CA6_B	2
CMD31			CA7_A	CA7_B	2
CMD19			CA8_A	CA8_B	2
CMD17			CA9_A	CA9_B	2
CMD22			CAB1_A	CAB1_B	2



PLL AVDD		
Valule	NV Q'ty	LCFC Q'ty
1uF	Under 3	Under 4
4.7uF	Near 2	Near 2
22uF	Near 1	Near 1
Beed : 30ohm/100Mhz (ESR=0.01ohm)		

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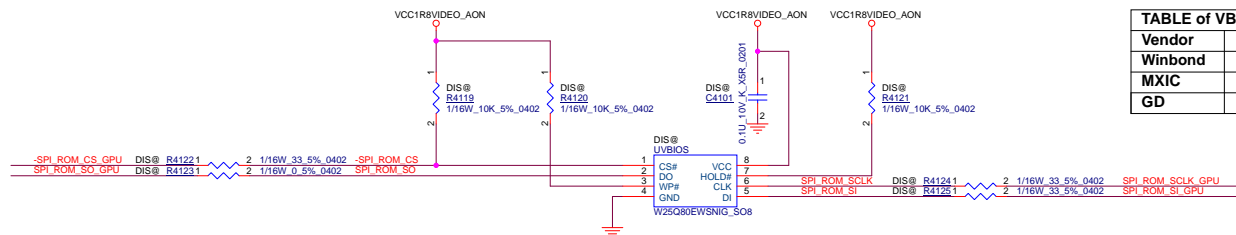
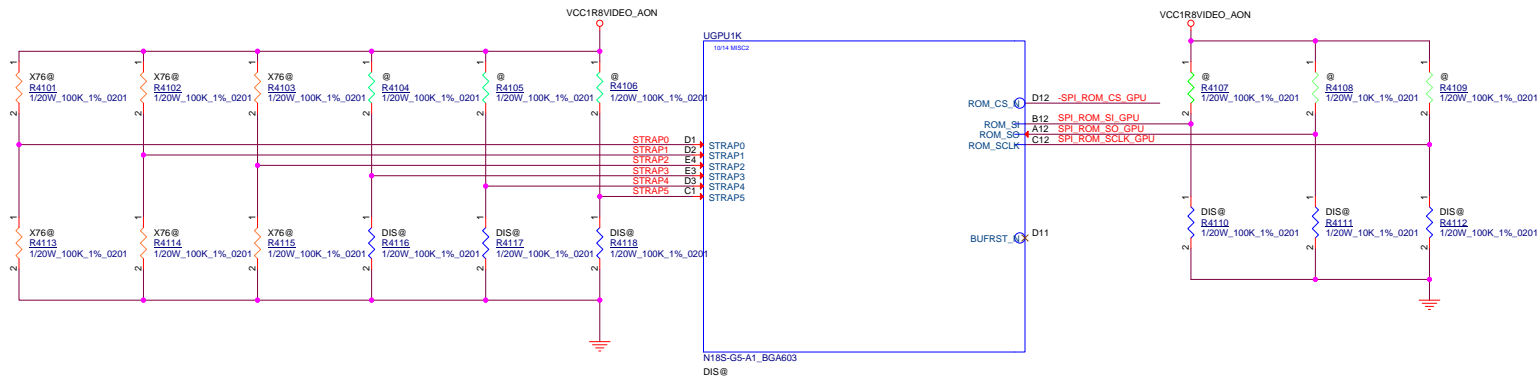


TABLE of VBIOS ROM (UVBIOS)		
Vendor	LCFC P/N	Description
Winbond	SA000080E00	S IC FL 8M W25Q80EWSNIG SOIC 8P SPI ROM
MXIC	SA00009WK00	S IC FL 8M MX25U8035FM11 SOP 8P
GD	SA000086910	S IC FL 8M GD25LQ80CTIGR SOP 8P 150MIL

N18-G5 VX76 Config (VRAM + Resistance)

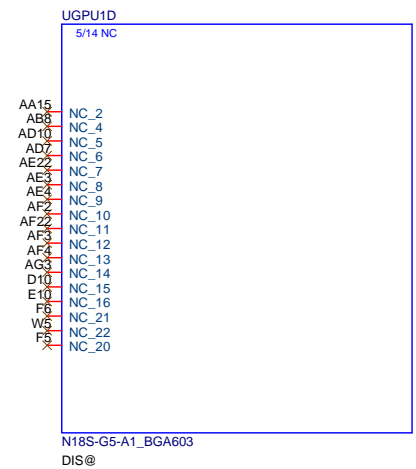
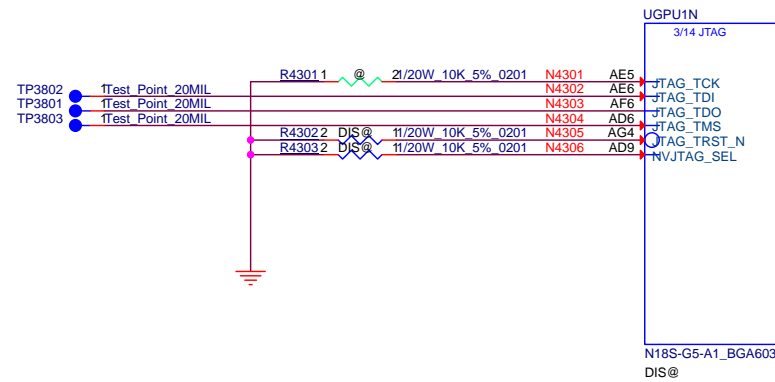
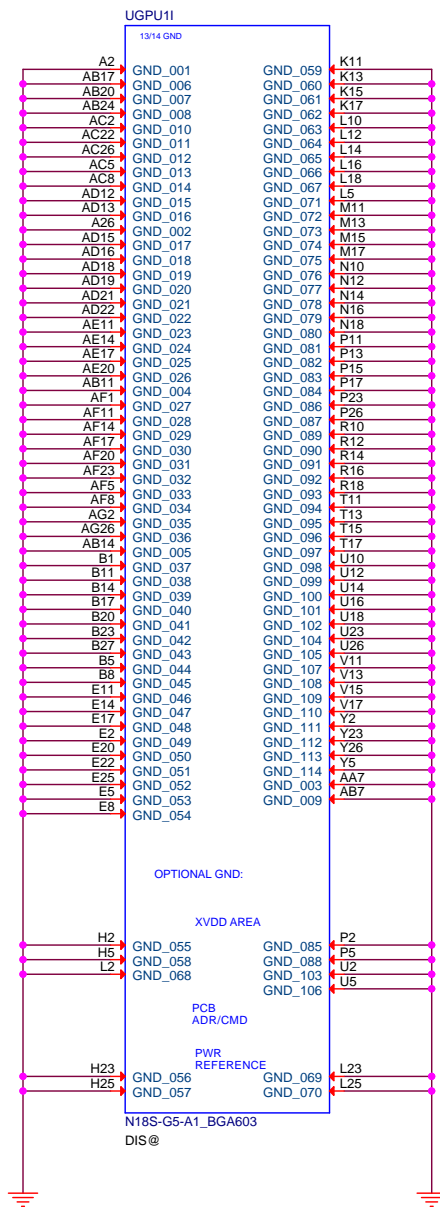
Memory Density	Vendor	Manufacturer P/N	RAMCFG Setting Number	STRAP 2		STRAP 1		STRAP 0	
				H R4103	L R4115	H R4102	L R4114	H R4101	L R4113
8Gb (256M x 32)	Micron A-die	MT61K256M32JE-14:A SA00009L510	1 (0x0001)	No ASM	ASM	No ASM	ASM	ASM	No ASM
	SAMSUNG C-die	K4Z80325BC-HC14 SA00009L410	0 (0x0000)	No ASM	ASM	No ASM	ASM	No ASM	ASM
	Hynix A-die	H56C8H24AIR-S2C SA0000B4E00	2 (0x0010)	No ASM	ASM	ASM	No ASM	No ASM	ASM


Table 12. N185-G5-B, N185-G5 and N185-LP GDDR6 Recommended Memories

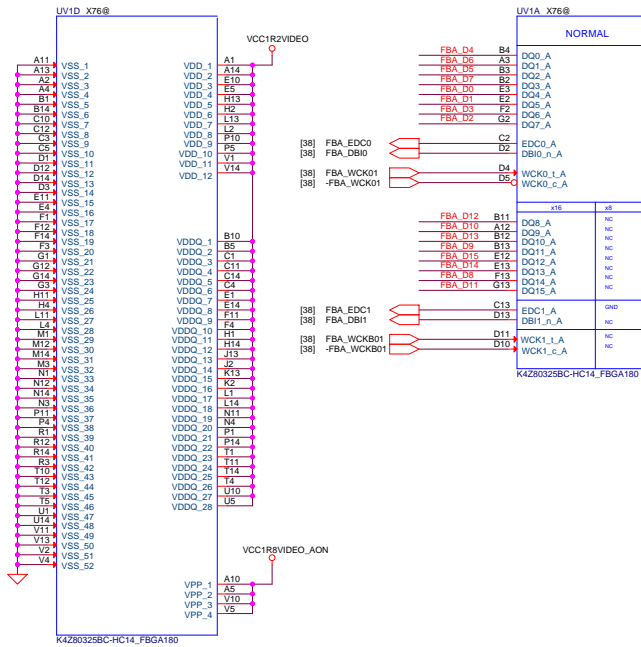
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 ²	Full	Production ready
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ³	Full	Production ready
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production ready

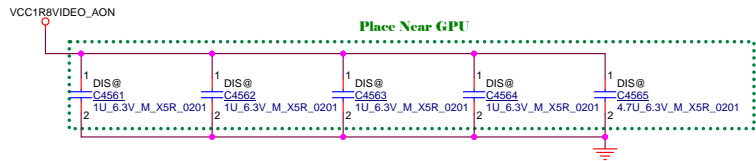
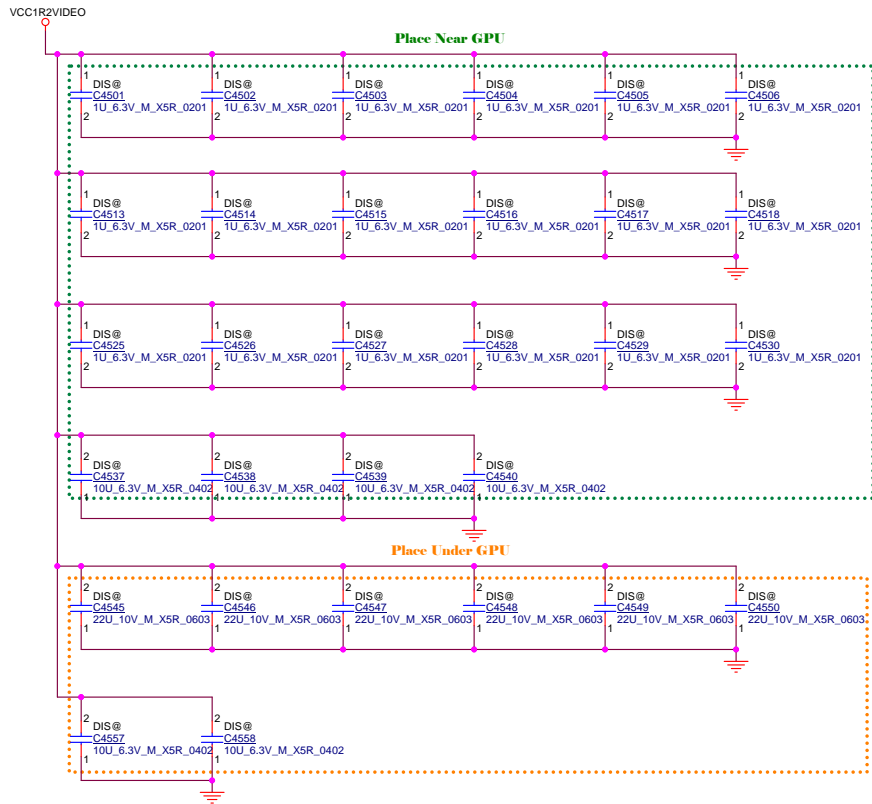
Table 11.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	L	8 (0x0008)	
L	L	H	9 (0x0009)	
L	H	L	10 (0x000A)	
L	H	H	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	



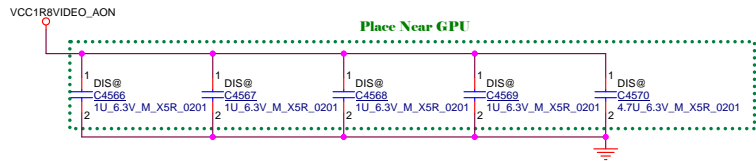
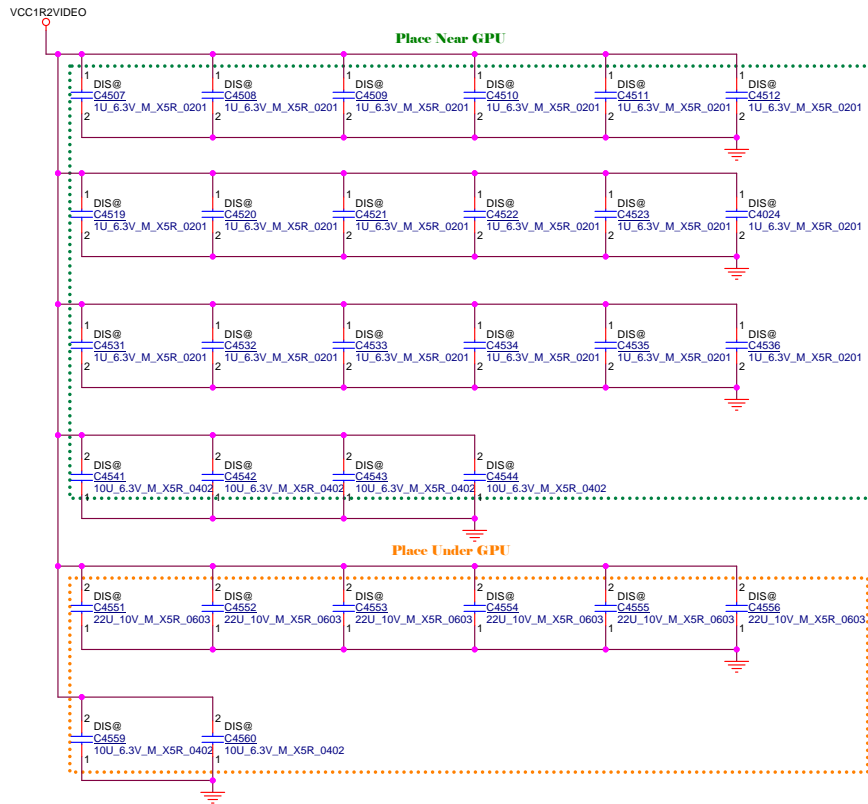
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VDD/VDDQ		
Valule	NV Q'ty	LCFC Q'ty
1uF	Near 18	Near 18
10uF	Near 4	Near 4
10uF	Under 2	Under 2
22uF	Under 6	Under 6


VPP		
Valule	NV Q'ty	LCFC Q'ty
1uF	Near 4	Near 4
4.7uF	Near 1	Near 1



VDD/VDDQ		
Valule	NV Q'ty	LCFC Q'ty
1uF	Near 18	Near 18
10uF	Near 4	Near 4
10uF	Under 2	Under 2
22uF	Under 6	Under 6


VPP		
Valule	NV Q'ty	LCFC Q'ty
1uF	Near 4	Near 4
4.7uF	Near 1	Near 1

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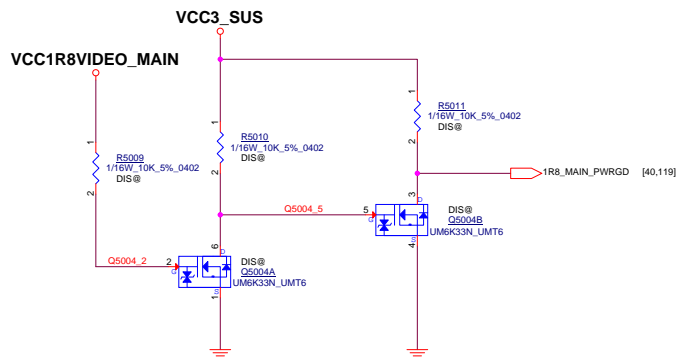
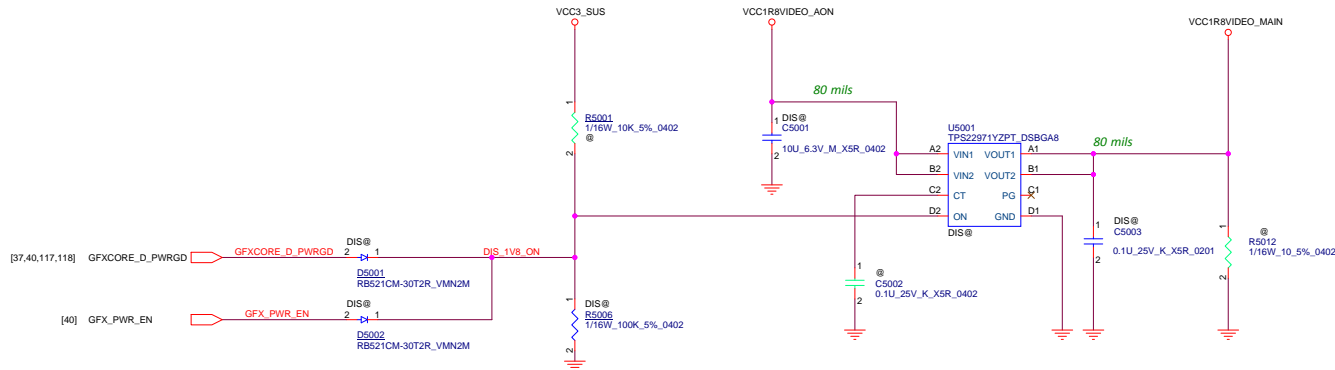
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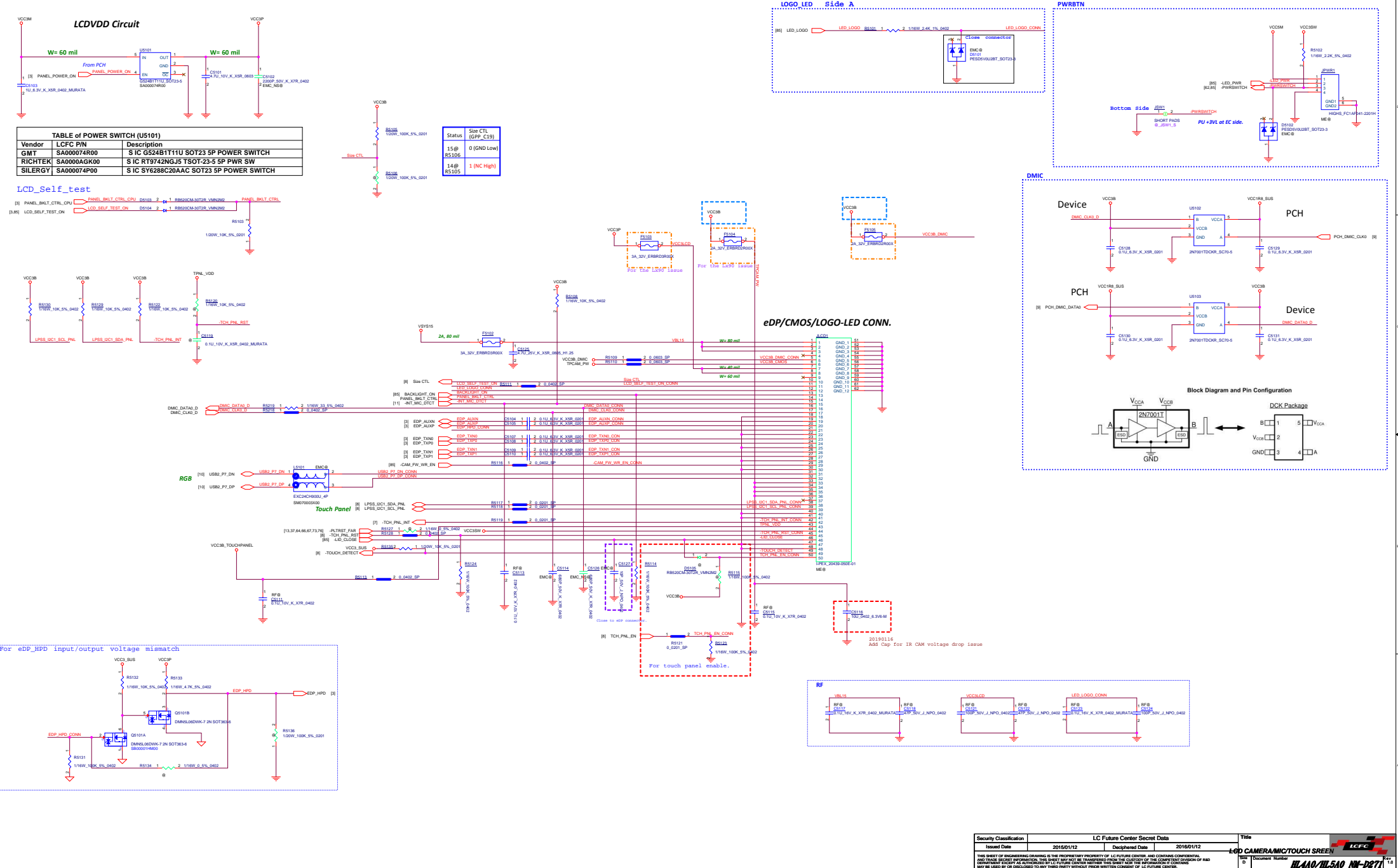
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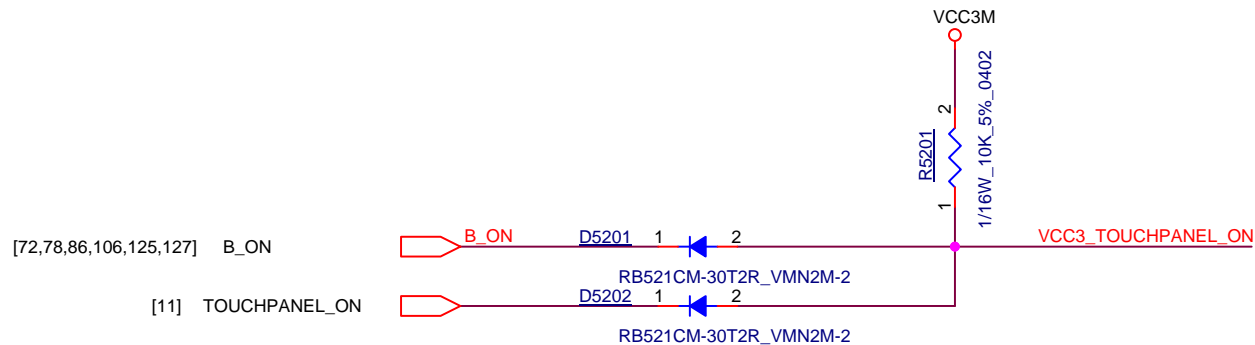
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VCC1R8VIDEO_MAIN VCC1R8VIDEO_MAIN [37,38,39]

VCC1R8_SUS to VCC1R8VIDEO_MAIN / VCC1R8VIDEO_MEM

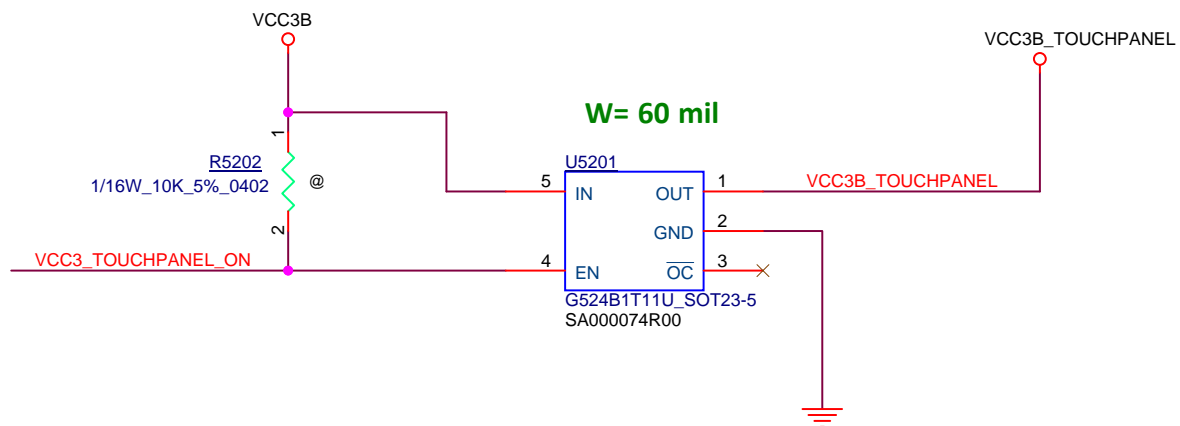


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Touch@ for MODS Touch panel

TABLE of POWER SWITCH (U5201)

Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
RICHTEK	SA0000AGK00	S IC RT9742NGJ5 TSOT-23-5 5P PWR SW
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

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VCC3B VCC3B [3,7,8,10,12,13,33,34,35,36,37,51,52,55,57,58,63,64,66,67,70,73,76,78,85,88,89,91,92,93,98,101,127]

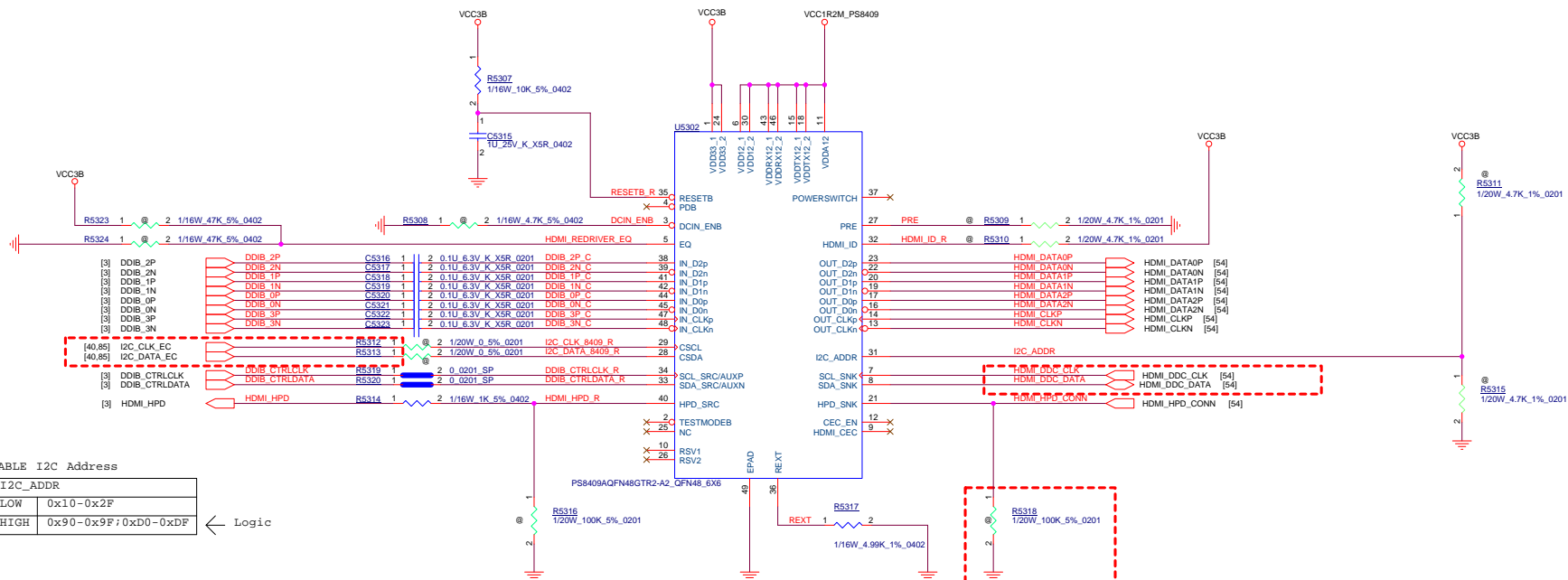
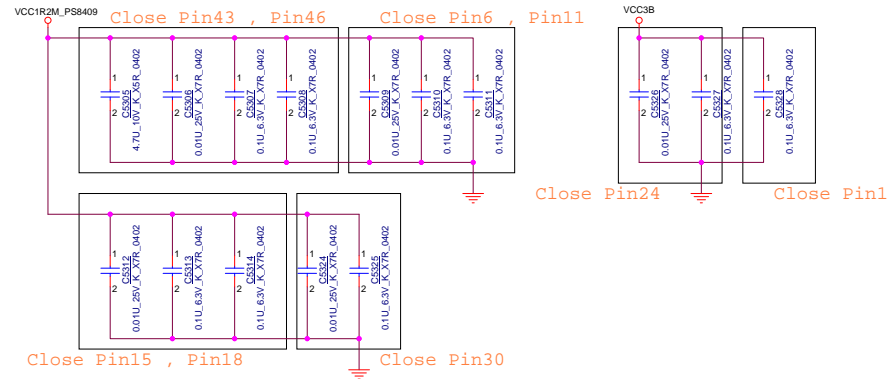
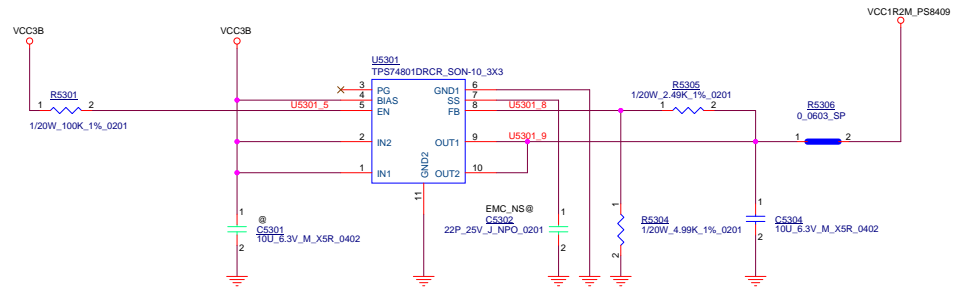
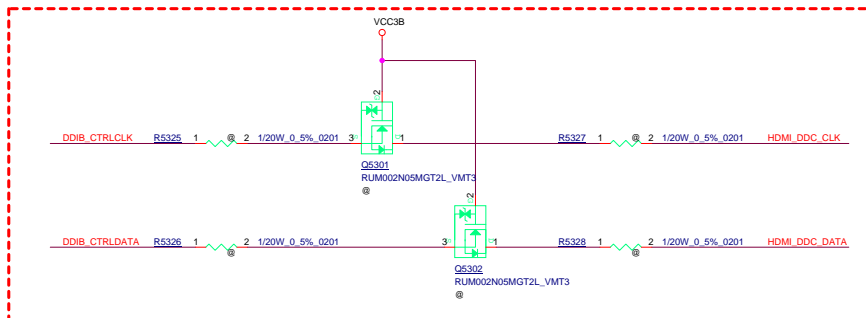


TABLE I2C Address

I2C_ADDR	
LOW	0x10-0x2F
HIGH	0x90-0x9F/0xD0-0xDF

← Logic



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Title			Rev
HDMI Re-Timer			
Size C	Document Number	HL4A0/HL5A0 NM-D271	1.0
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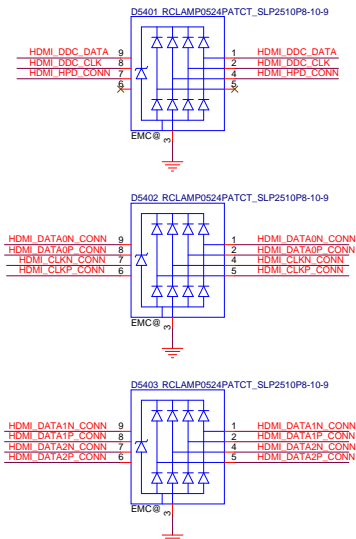
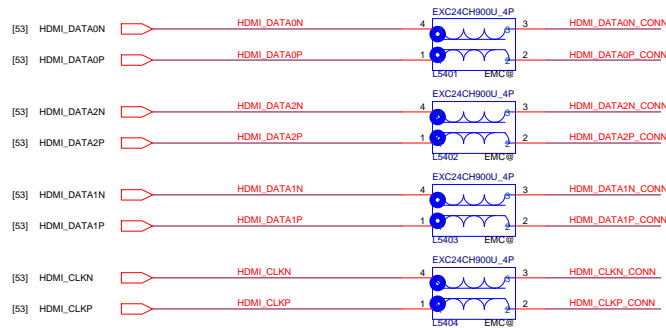
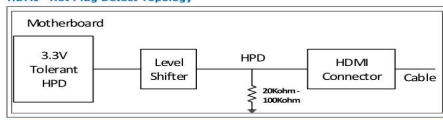
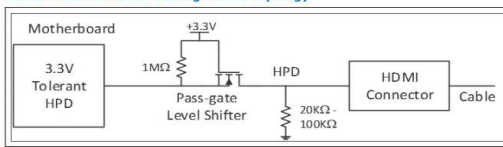


Figure 57. HDMI* Hot Plug Detect Topology



- NOTE**
- Recommend 50 ohm nominal trace impedance with reasonable noise isolation.
 - Ensure necessary protection circuitry is in place to prevent back-drive current from damaging the processor when the sink device is powered off.

Figure 58. HDMI* Cost Reduced Hot Plug Detect Topology



- NOTE**
- Recommend 50 ohm nominal trace impedance with reasonable noise isolation.

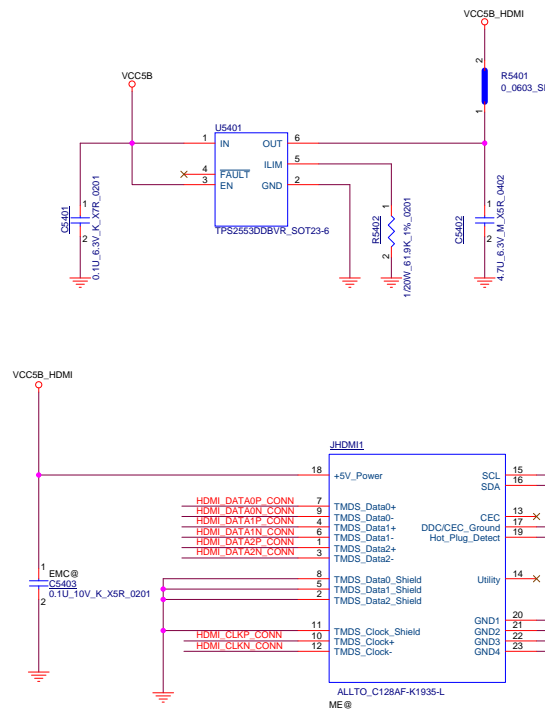
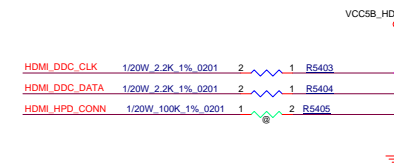
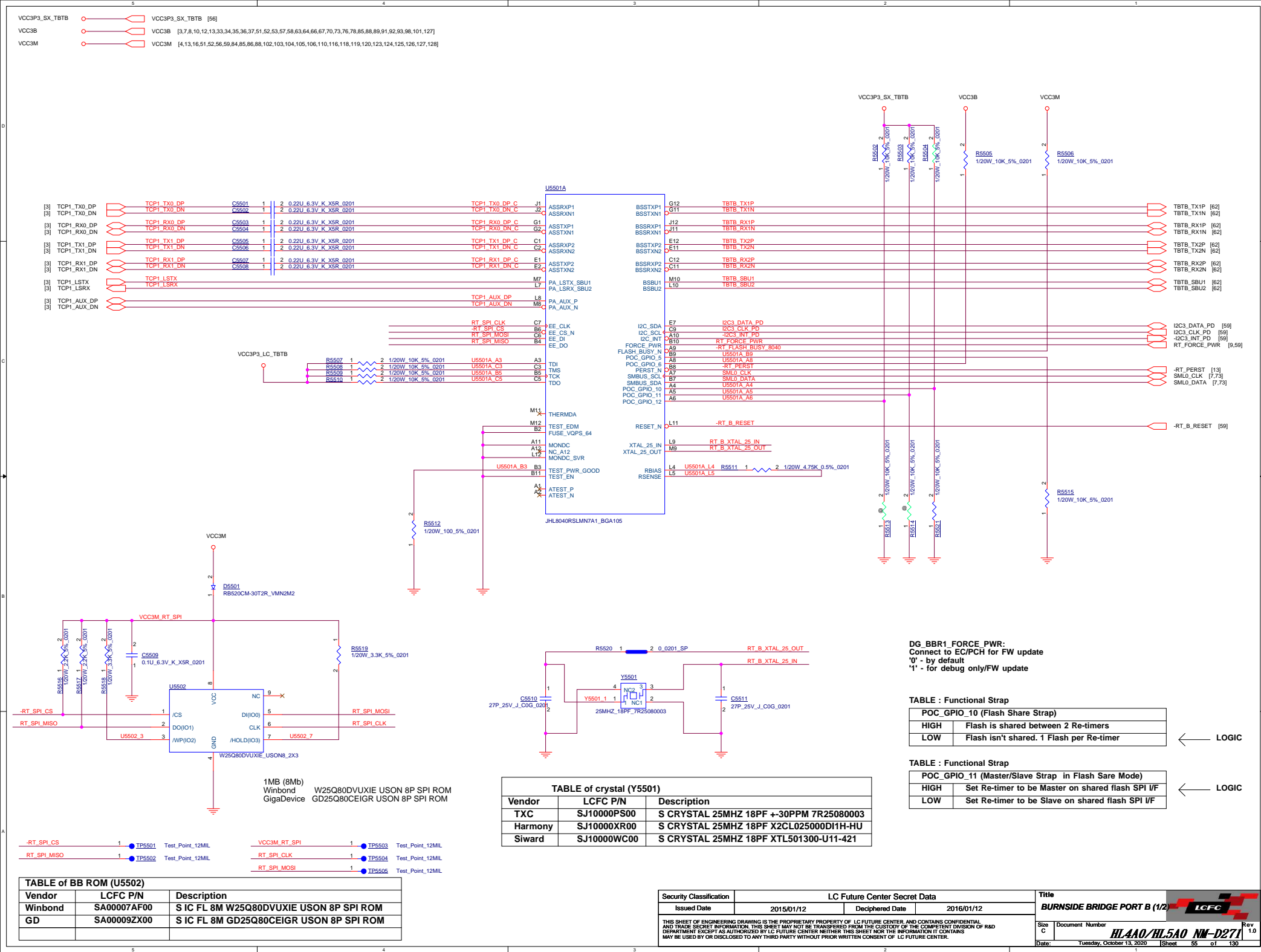
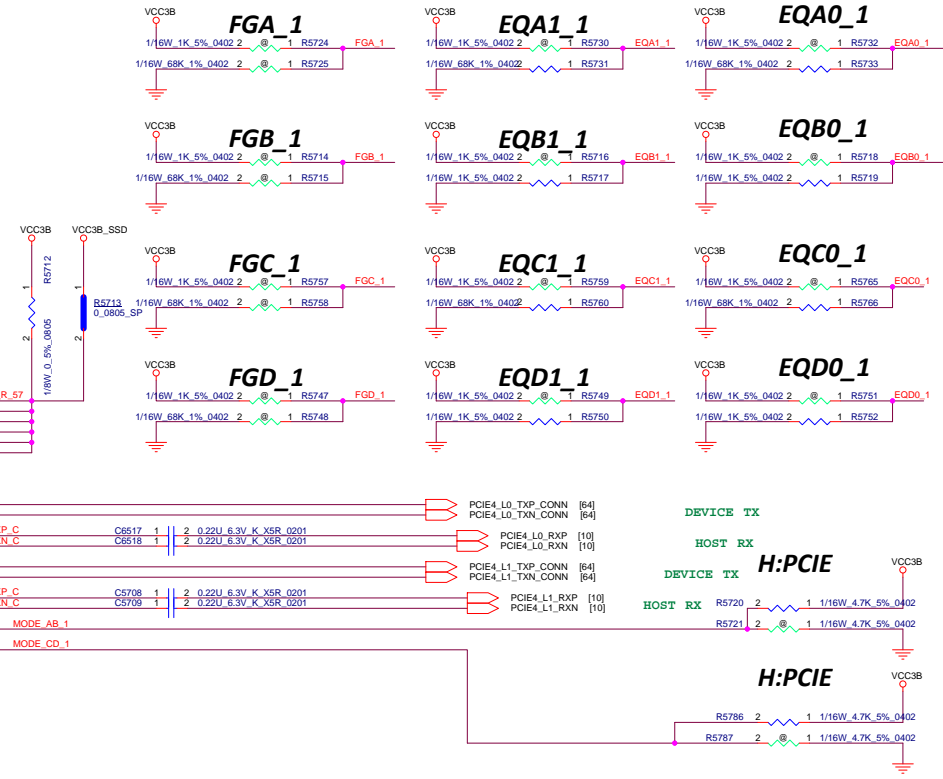
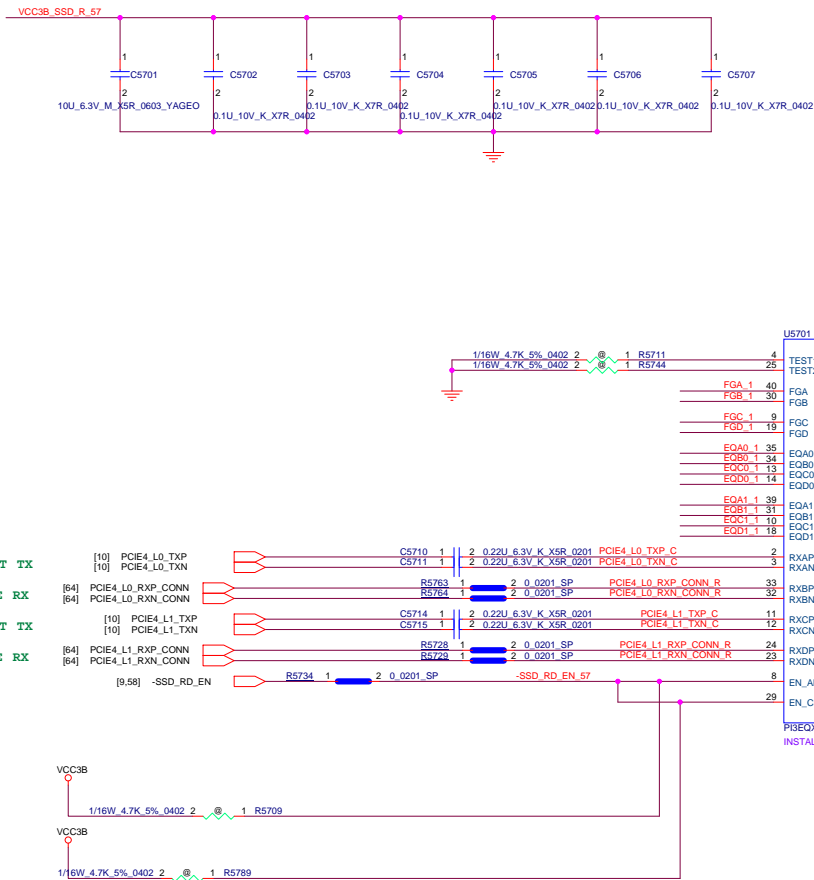


TABLE of Transformer (U5401)		
Vendor	LCFC P/N	Description
TI	SA00008F300	S IC TPS2553DDBVR SOT-23 6P USB POWER SW
GMT	SA00007CY00	S IC G517AL1TB1U SOT-23 6P HDMI POWER SW
DII	SA00008NJ00	S IC AP2553W6-7 SOT-26 6P USB POWER SW







Equalization Setting:

EQA/B are the selection pins for the equalization selection

EQ		Equalizer setting (dB)			
A1/B1	A0/B0	@1.25GHz	@2.5GHz	@3GHz	@4GHz
0	0	0.4	1.8	2.4	3.9
0	R	0.6	2.3	3.2	4.9
0	F	0.8	2.9	3.9	5.8
0	1	1.0	3.5	4.6	6.6
R	0	2.1	4.4	5.3	7.2
R	R	2.3	4.9	5.9	7.9
R	F	2.5	5.3	6.4	8.5
R	1	2.7	5.8	7.0	9.1
F	0	3.7	6.5	7.7	9.7
F	R	3.9	6.9	8.1	10.2
F	F	4.1	7.3	8.5	10.6
F	1	4.3	7.6	8.9	11.0
1	0	5.4	8.4	9.5	11.4
1	R	5.6	8.7	9.8	11.8
1	F	5.8	9.0	10.2	12.1
1	1	5.9	9.2	10.4	12.5

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

Flat Gain Settings	
FGA/B	dB
0	-3.5
R	-1.5
F	0 (Default)
1	+1.5

-1dB compression point output Swing Setting:

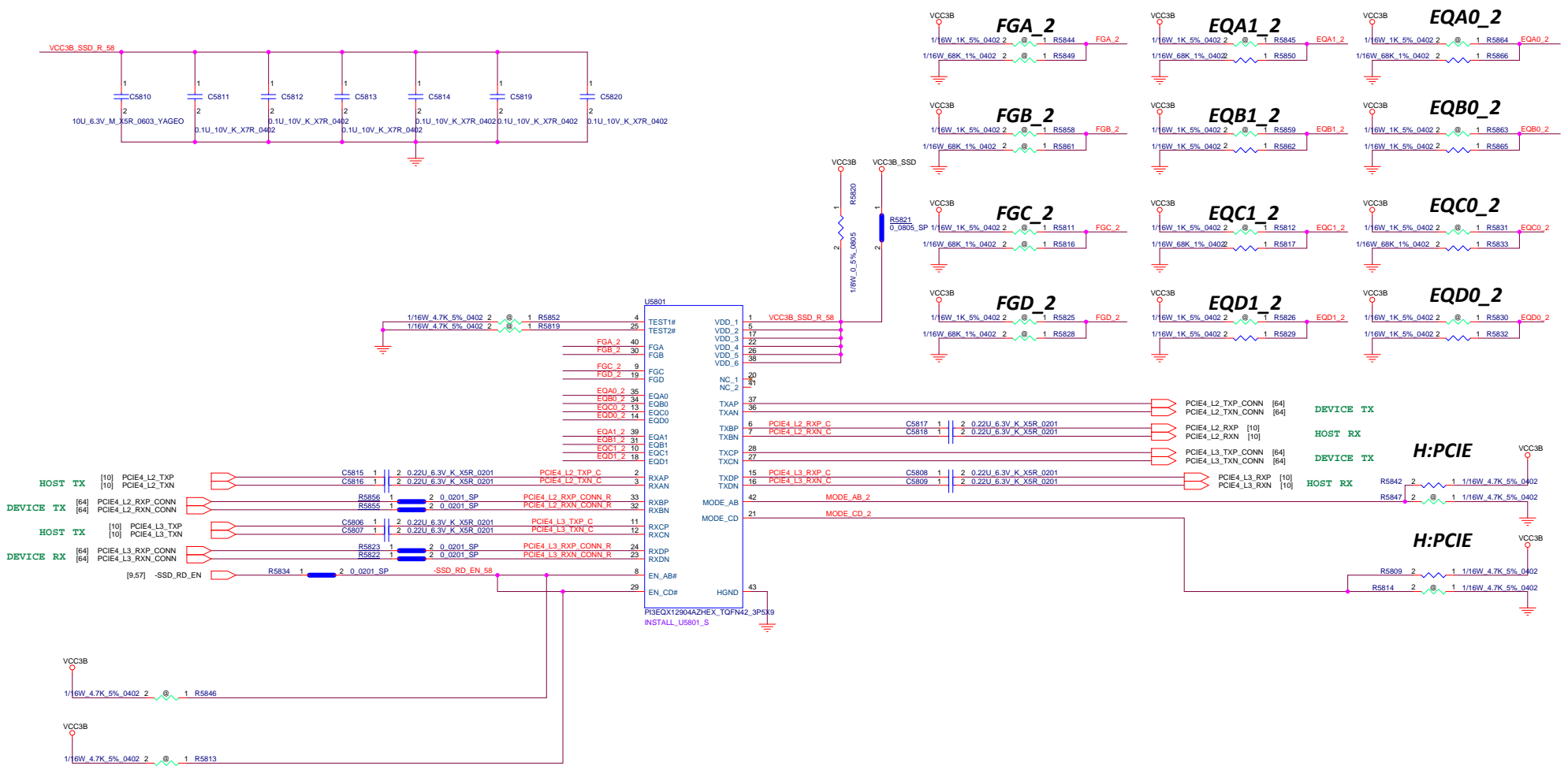
SWA/B are the selection bits for the -1dB compression point output swing setting (100Mhz)

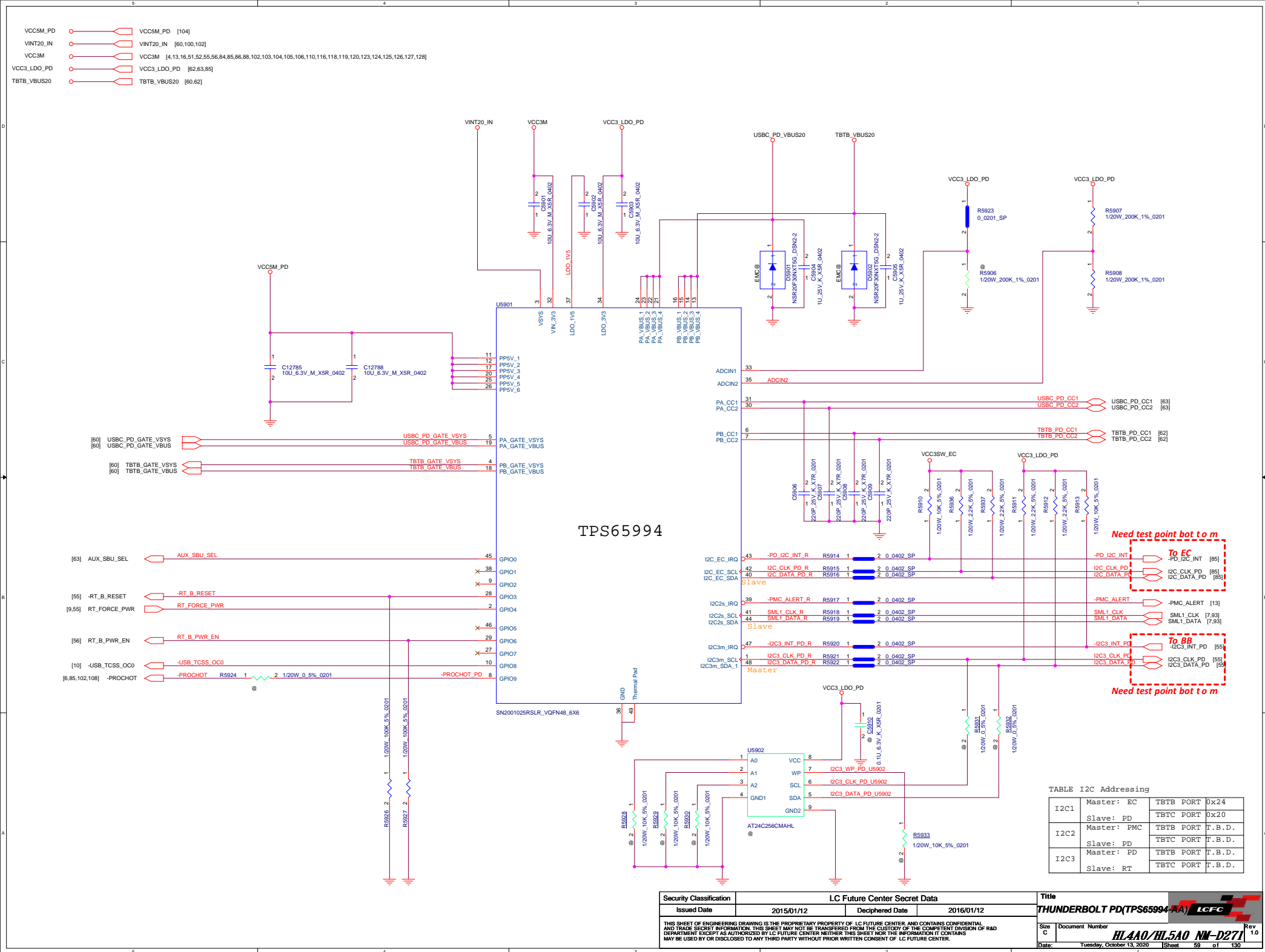
Output Linear Swing Settings	
SWA/B	mVppd
0	990
R	1050
F	1000 (Default)
1	1120

EL480/580 Setting					
TX EQ	TX SW	TX Gain	RX EQ	RX SW	RX Gain
A1:R A0:F	1	F	B1:0 B0:1	1	F
TX EQ	TX SW	TX Gain	RX EQ	RX SW	RX Gain
A1:R A0:F	1	F	B1:0 B0:1	1	F

Channel Enable Setting	
EN#	Setting
0	Enabled (Default)
1	Disabled

Channel Enable Setting	
EN#	Setting
0	Enabled (Default)
1	Disabled





TPS65994

Need test point bot t o m

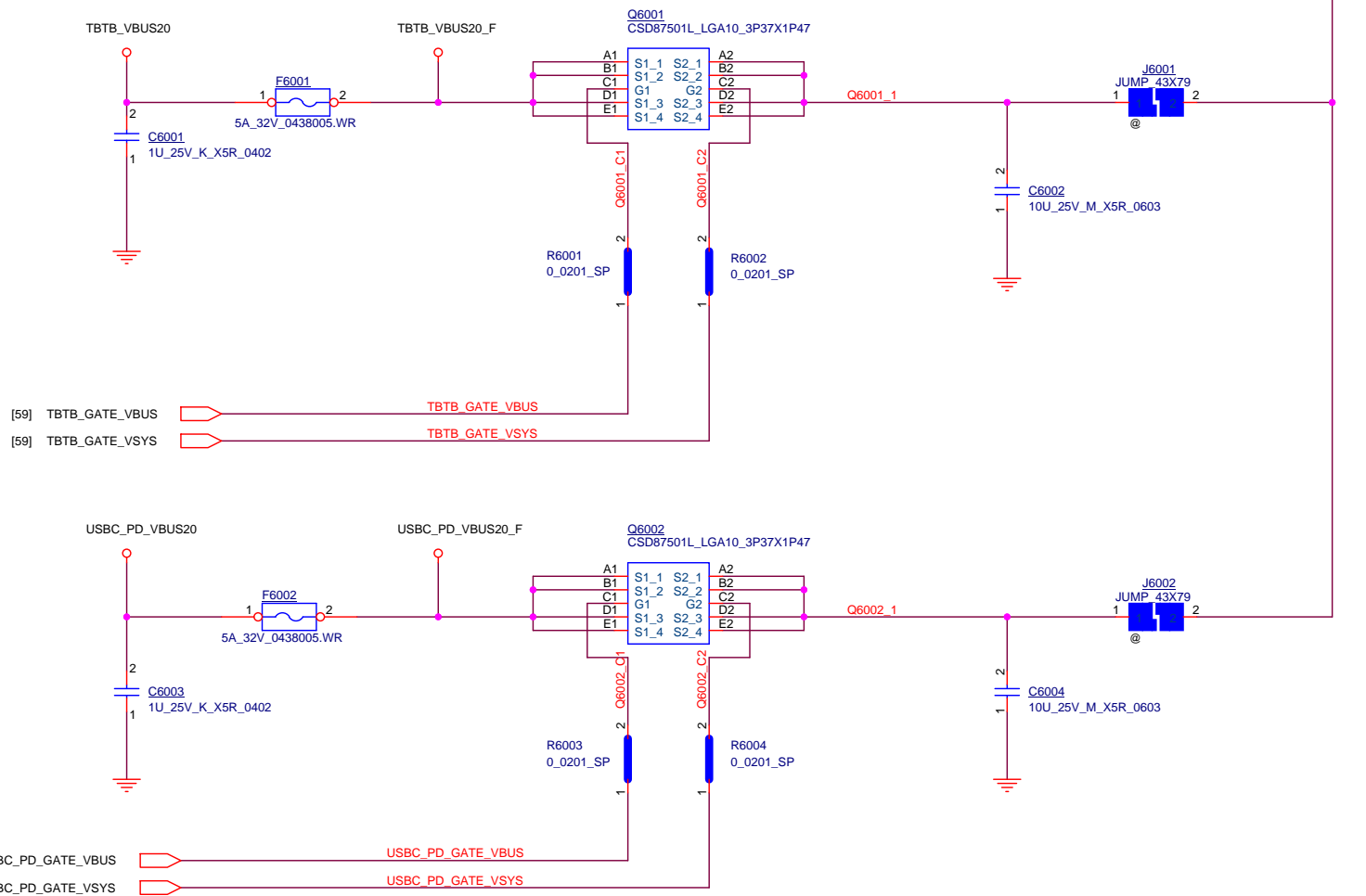
To EC


To BB

Need test point bot t o m


TABLE I2C Addressing			
I2C1	Master:	EC	TBTB PORT 0x24
	Slave:	PD	TBTC PORT 0x20
I2C2	Master:	PMC	TBTB PORT T.B.D.
	Slave:	PD	TBTC PORT T.B.D.
I2C3	Master:	PD	TBTB PORT T.B.D.
	Slave:	RT	TBTC PORT T.B.D.

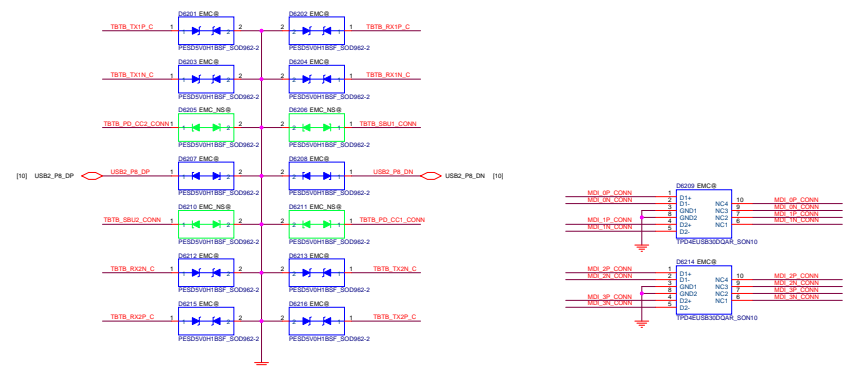
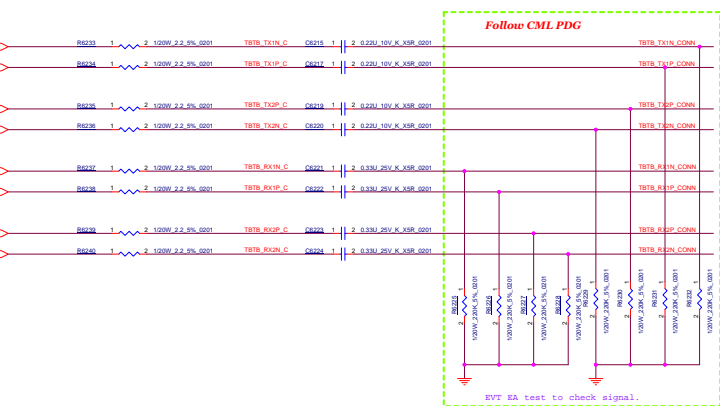
VINT20_IN [59,100,102]
TBTB_VBUS20 [59,62]
USBC_PD_VBUS20 [59,63]
TBTB_VBUS20_F
USBC_PD_VBUS20_F




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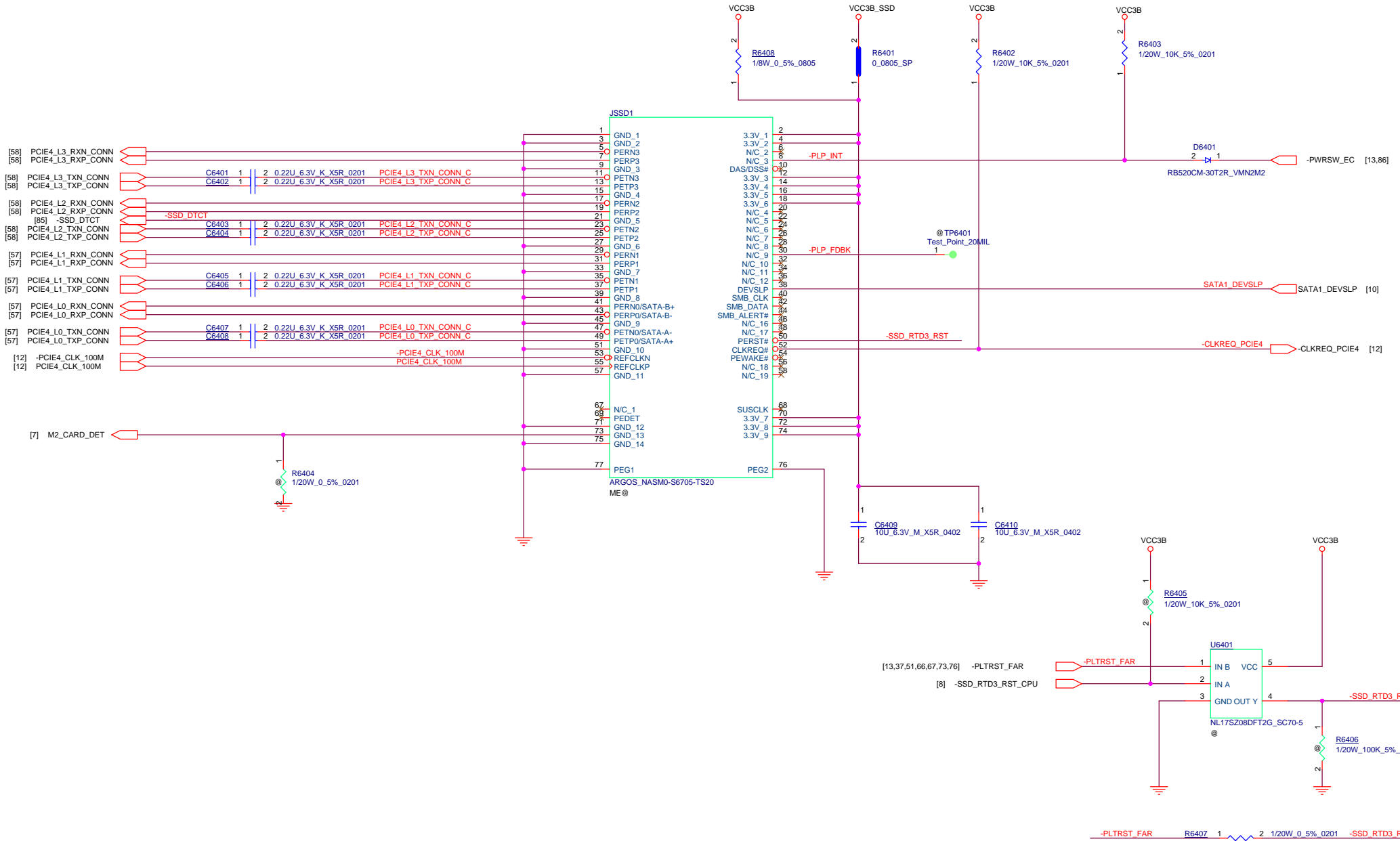
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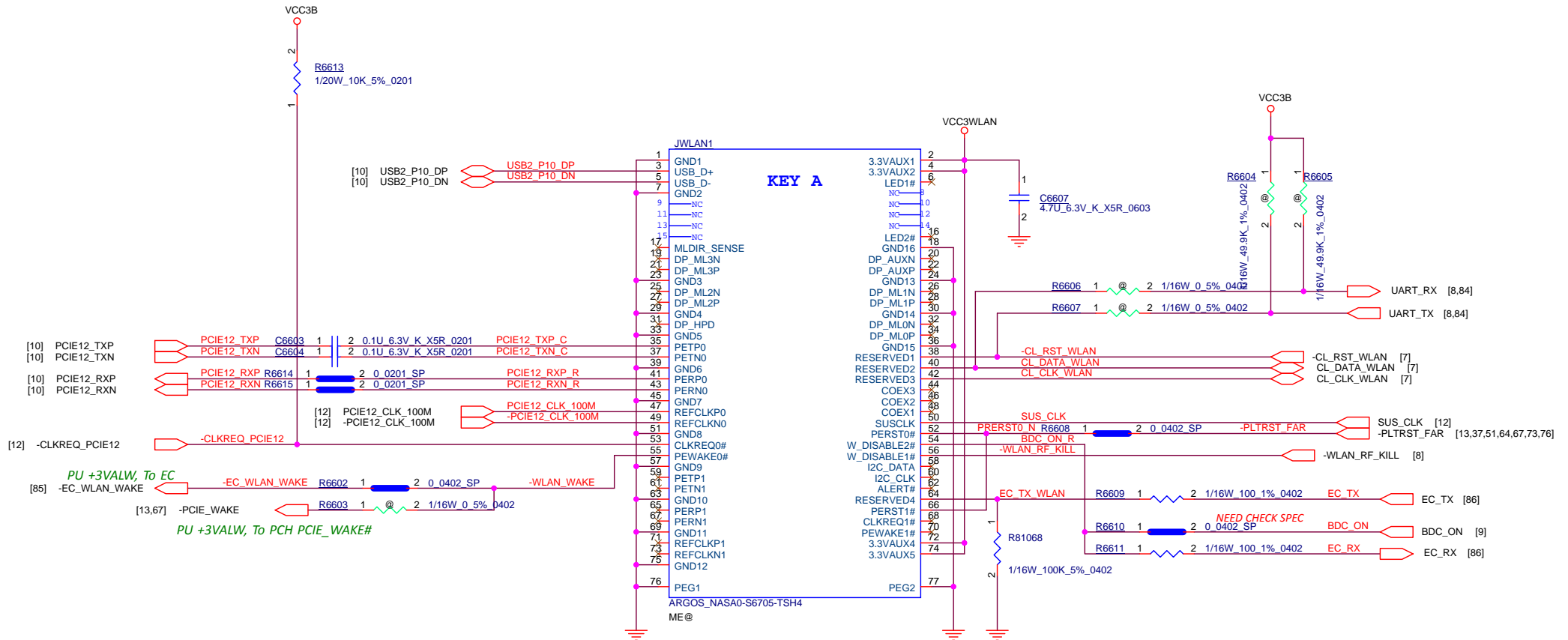



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VCC3B VCC3B [3,7,8,10,12,13,33,34,35,36,37,51,52,53,55,57,58,63,64,67,70,73,76,78,85,88,89,91,92,93,98,101,127]

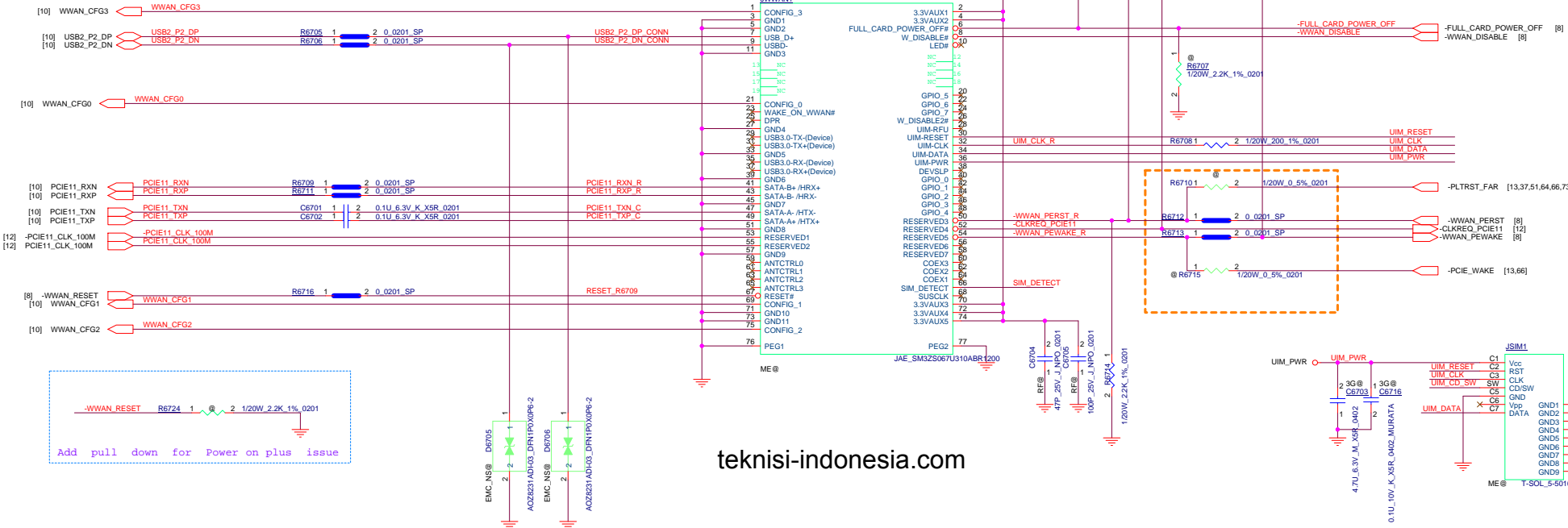


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GND	51
PERp0/SATA-A+	49
PERn0/SATA-A-	47
GND	45
PETp0/SATA-B-	43
PETn0/SATA-B+	41
GND	39
PERp1/USB3.0-Rx+/SSIC-RxP	37
PERn1/USB3.0-Rx-/SSIC-RxN	35
GND	33
PETp1/USB3.0-Tx+/SSIC-TxP	31
PETn1/USB3.0-Tx-/SSIC-TxN	29
GND	27
Reserved (Future Expansion)	25
Reserved (Future Expansion)	23
WWAN/SSD IND (GND-WWAN/OC-SSD)	21

M.2 Socket 2 (Key-B) for 3042 S3 WWAN

H=2.00mm Connector



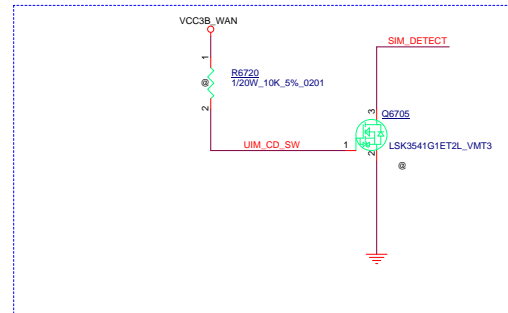
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TABLE:	Module Configuration Decodes				Module Type and Main Host Interface	Module
State #	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
	GND	GND	NC	NC	WWAN - PCIe, USB 3.1 Gen1	Quectel EM120R


Table 27: List of EM120R-GL Configuration Pins

Pin No.	Pin Name	Power Domain	Description
21	CONFIG_0	0	Connected to GND internally.
69	CONFIG_1	0	Connected to GND internally.
75	CONFIG_2	0	NC
1	CONFIG_3	0	NC

20181114
Add mos for SIM_DETECT function



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VCC5M [51,70,72,84,85,103,107,108,109,110,116,117,118,119,120,125,126,127]
USB_PWR_S2 USB_PWR_S2

USB AOU

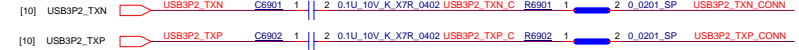
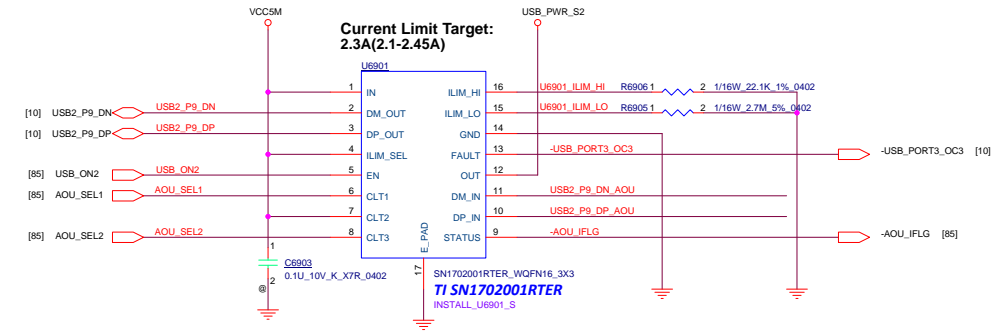
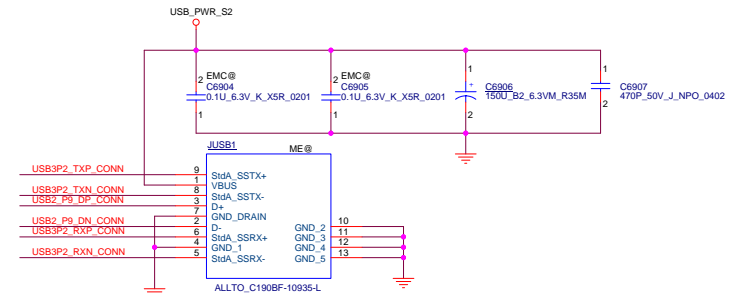
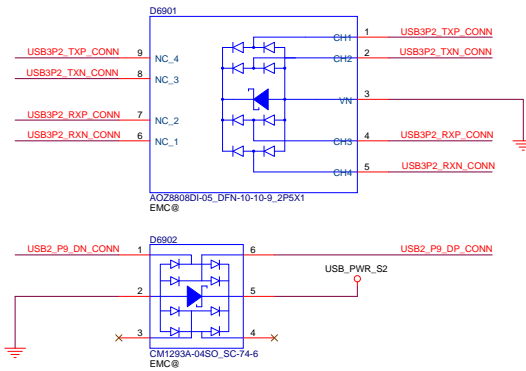
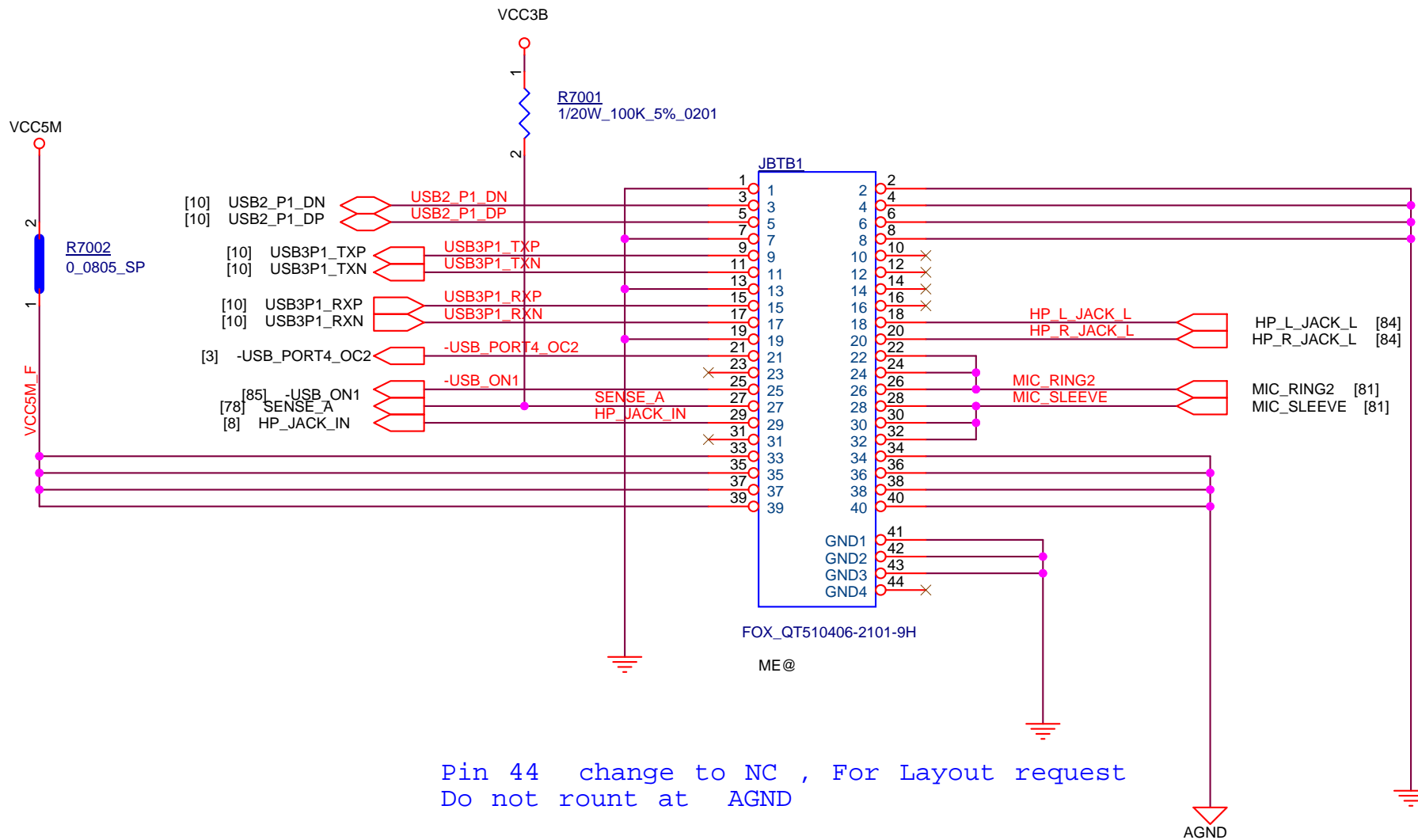


TABLE of POWER SWITCH (U6901)		
Vendor	LCFC P/N	Description
TI	SA00008HF00	S IC SN1702001RTER WQFN 16P USB CHARGING
PERICOM	SA00009D800	S IC PI5USB2546HZHEX TQFN 16P CONTROLLER

CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
★	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
★	1	1	1	SDP2 Data Connected
★	1	1	0	SDP1 Data Connected
★	0	1	0	SDP1 Data Connected
	1	0	0	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
★	0	1	1	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
	0	0	1	DCP_Auto Data Disconnected and Power Wake Function Active





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USB TYPE-A CONNECTOR			
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Size	Document	Number	



Rev

SMART CARD CONN.

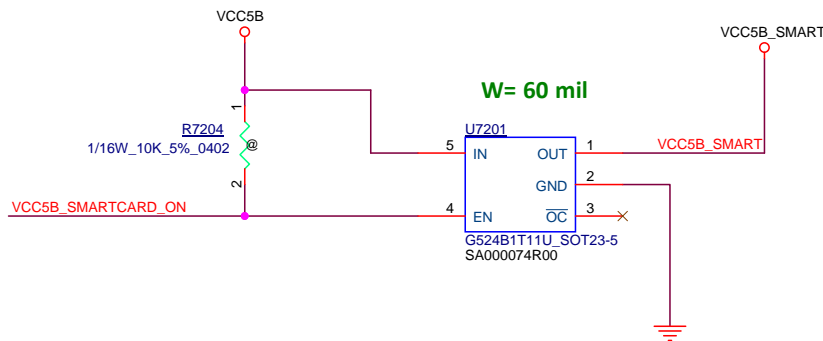
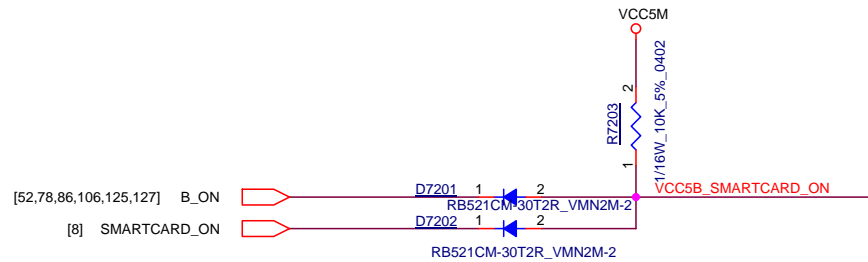
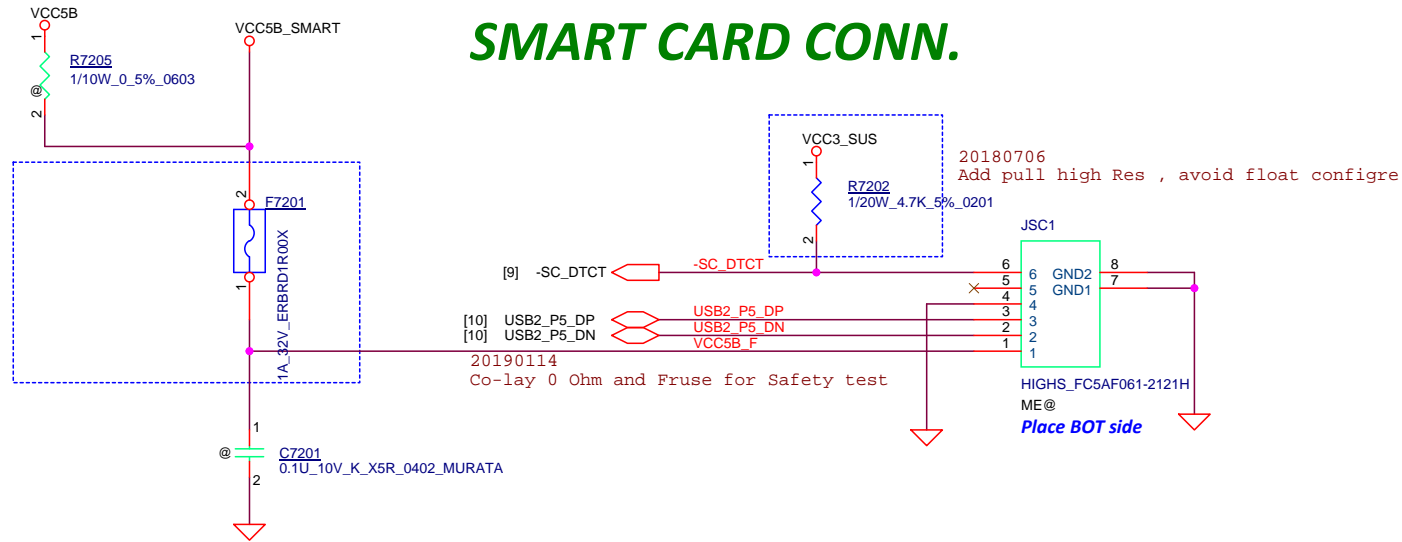
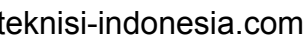


TABLE of POWER SWITCH (U7201)

Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
RICHTEK	SA0000AGK00	S IC RT9742NGJ5 TSOT-23-5 5P PWR SW
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

Smart@ for MODS Smart Card SKU



Title			
GBE JACKSONVILLE			
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VCC3GBE

VCC3GBE [73,75]

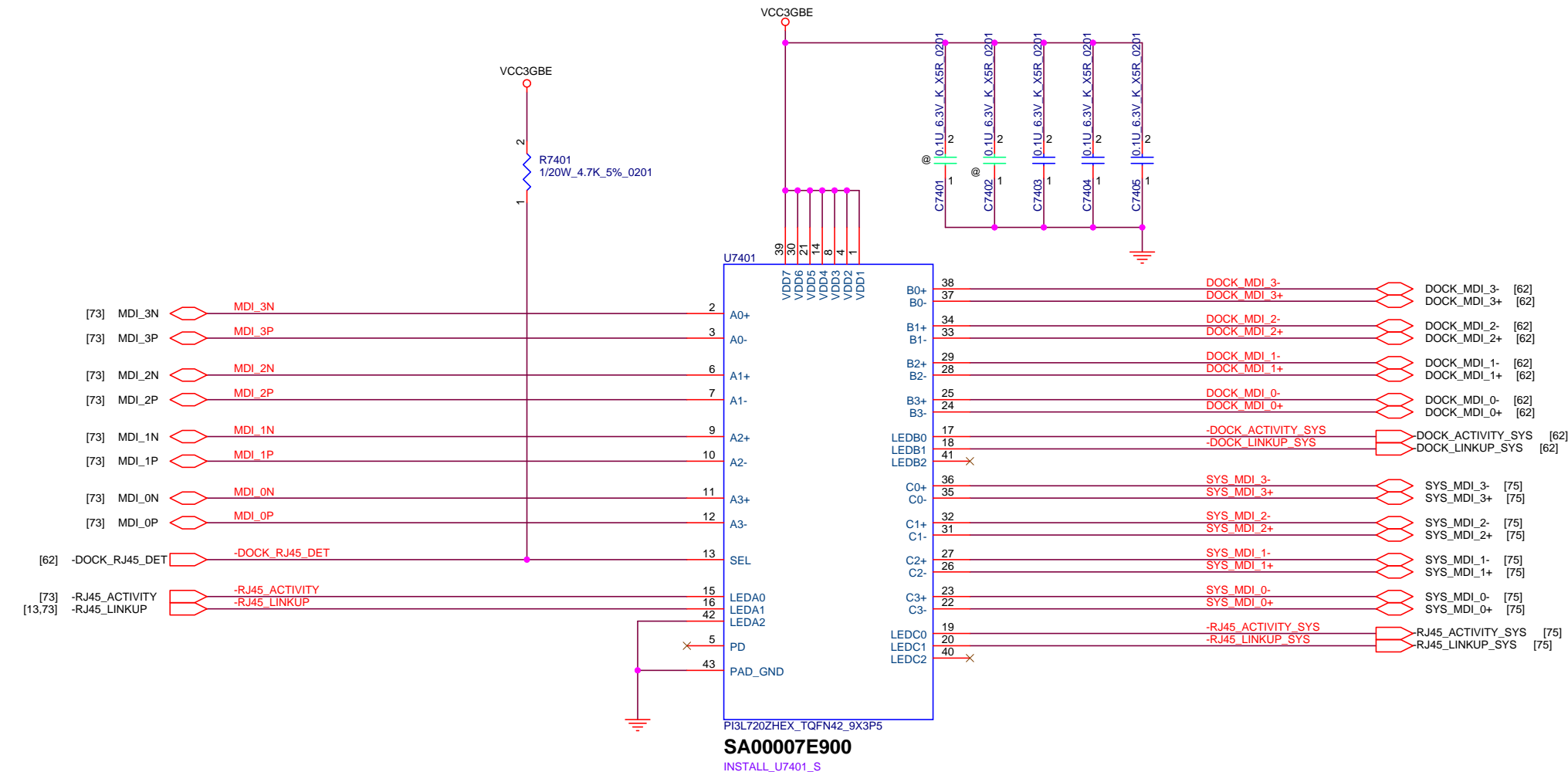


TABLE of LAN SWITCH (U7401)

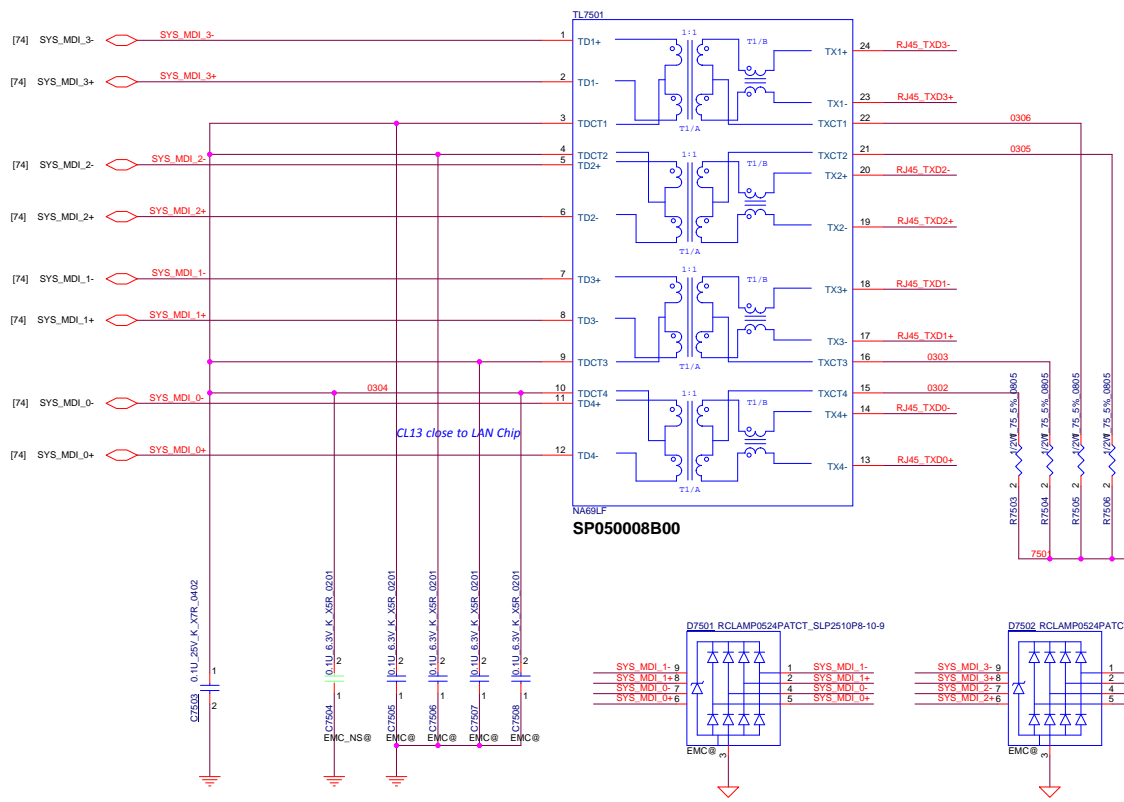
Vendor	LCFC P/N	Description
PERICOM	SA00007E900	S IC PI3L720ZHE+CX TQFN GBE LA
TI	SA000072400	S IC TS3L501ERUAR WQFN 42P LAN

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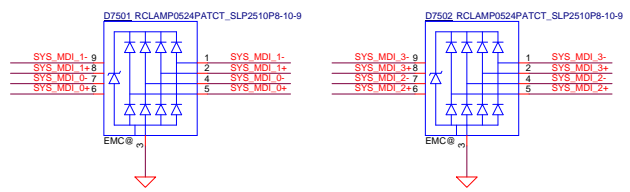
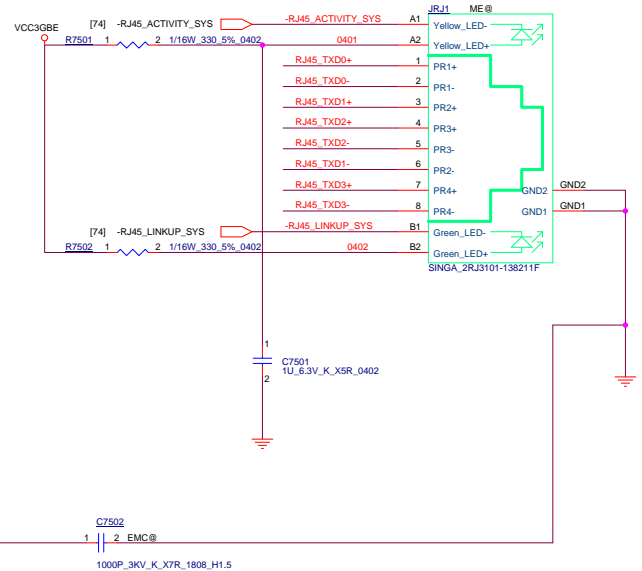
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LAN SWITCH		
Size	Document Number	Rev
Custom	HL4A0/HL5A0 NM-D271	1.0
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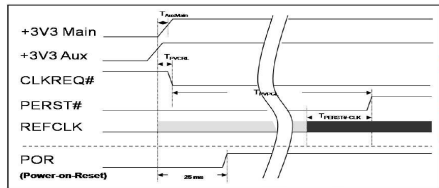
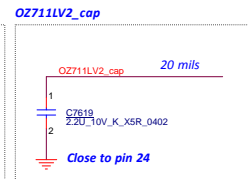
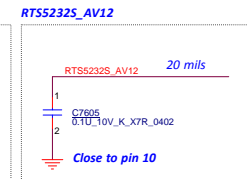
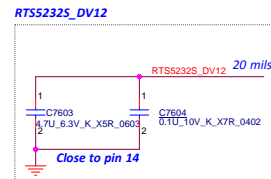
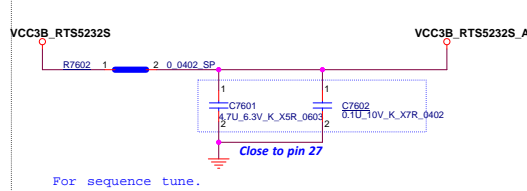
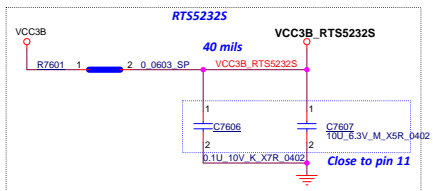
TABLE of Transformer (TL7501)		
Vendor	LCFC P/N	Description
BOTHHAND	SP050008B00	S X'FORM_ NA0069R LF LAN
TAIMAG	SP050009U00	S X'FORM_ IH-189-G LAN

LAN X' FORM

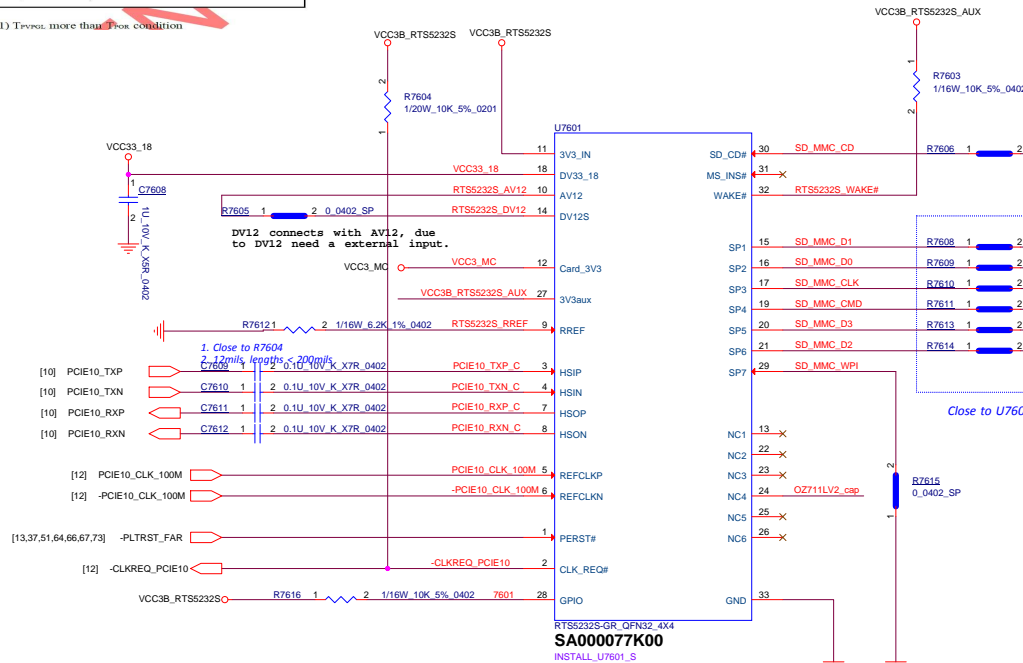


RJ45 Conn.

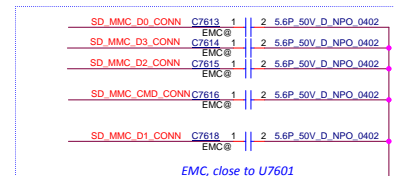




(1) T1000 more than 100ns condition



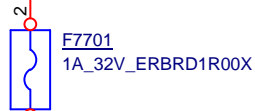
Part Number	Vendor
SA000077K00	RTS5232S-GR REALTEK
SA00009F600	OZ711LV2LN-A-0-TR



VCC3_MC

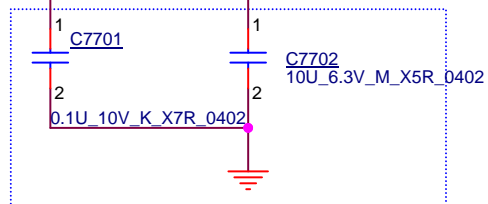
VCC3_MC [76]

VCC3_MC



40 mils

VCC3_MC_CONN



Close to JREAD1

[76] SD_MMC_D2_CONN
[76] SD_MMC_D3_CONN
[76] SD_MMC_CMD_CONN

SD_MMC_D2_CONN
SD_MMC_D3_CONN
SD_MMC_CMD_CONN

[76] SD_MMC_CLK_CONN

SD_MMC_CLK_CONN

[76] SD_MMC_D0_CONN
[76] SD_MMC_D1_CONN
[76] SD_MMC_CD_CONN

SD_MMC_D0_CONN
SD_MMC_D1_CONN
SD_MMC_CD_CONN

Mode	Detect
Normal	short
Card Insert	open

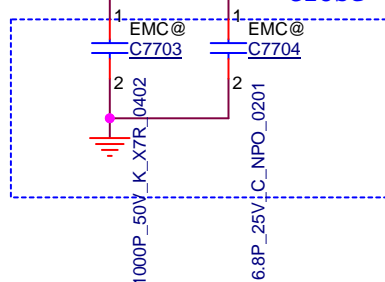
JREAD1


1 MICRO SD_DAT2
2 MICRO SD_CD/DAT3
3 MICRO SD_CMD
4 MICRO SD_VDDI
5 MICRO SD_CLK
6 MICRO SD_VSS
7 MICRO SD_DAT0/RCLK+
8 MICRO SD_DAT1/RCLK-
9 MICRO SD_CD

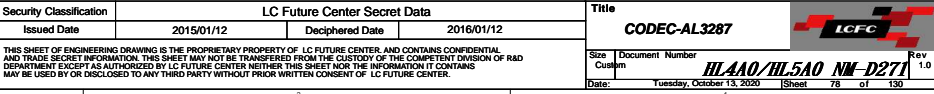
GND_1
GND_2
GND_3
GND_4

T-SOL_158-2220902601
ME@


Close to JREAD1

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				Date:	Tuesday, October 13, 2020	Sheet 77 of 130

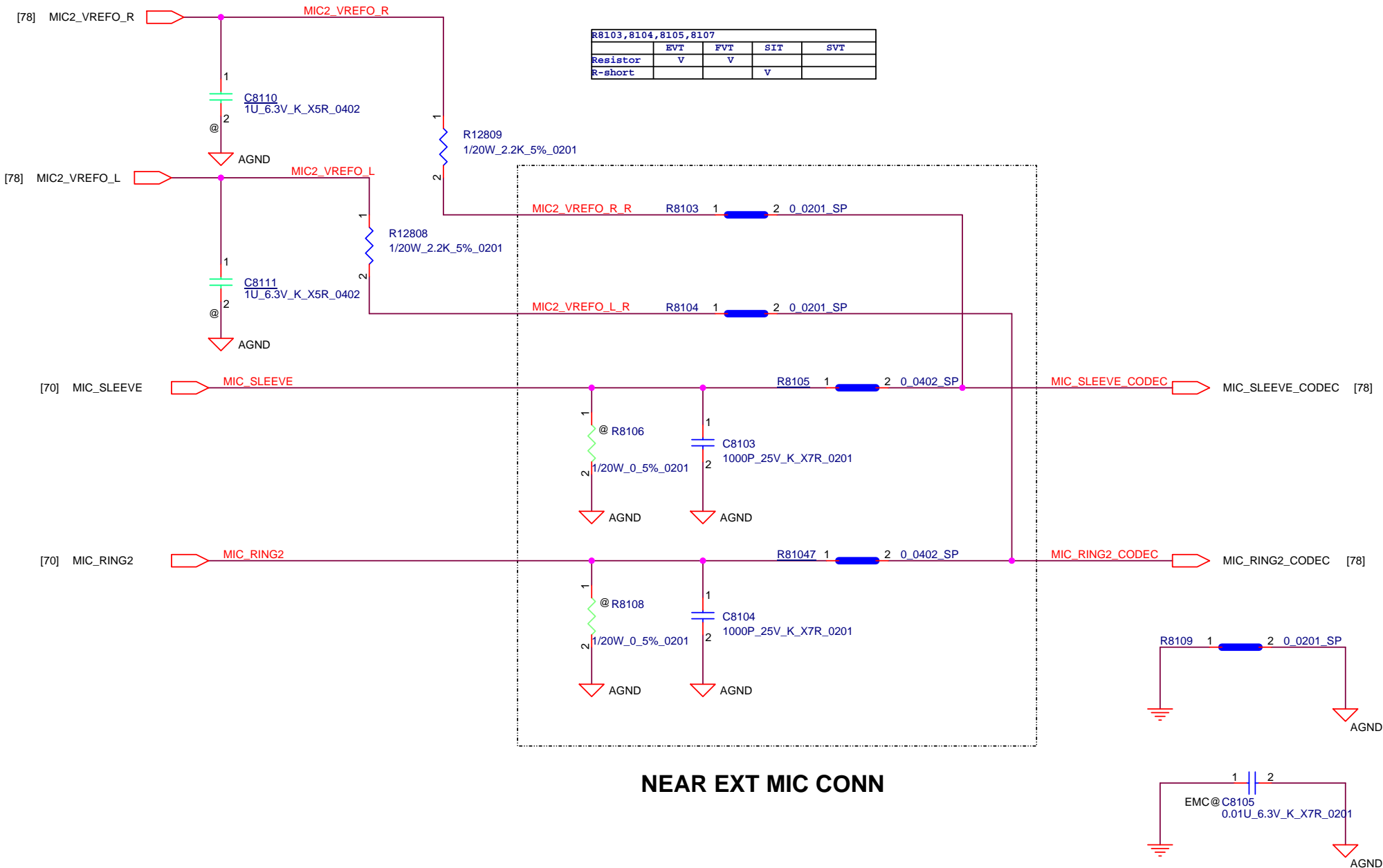


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Date: Tuesday, October 13, 2020				Sheet	79	of	130

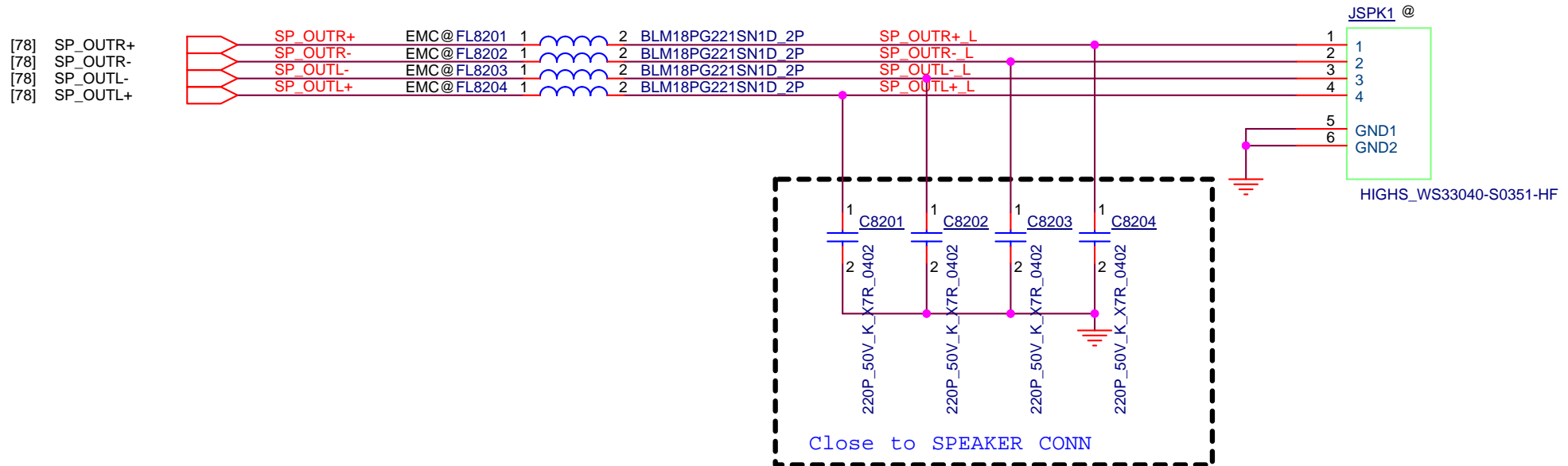
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	AUDIO JACK SENSE			
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Date: Tuesday, October 13, 2020				Sheet	80	of	130



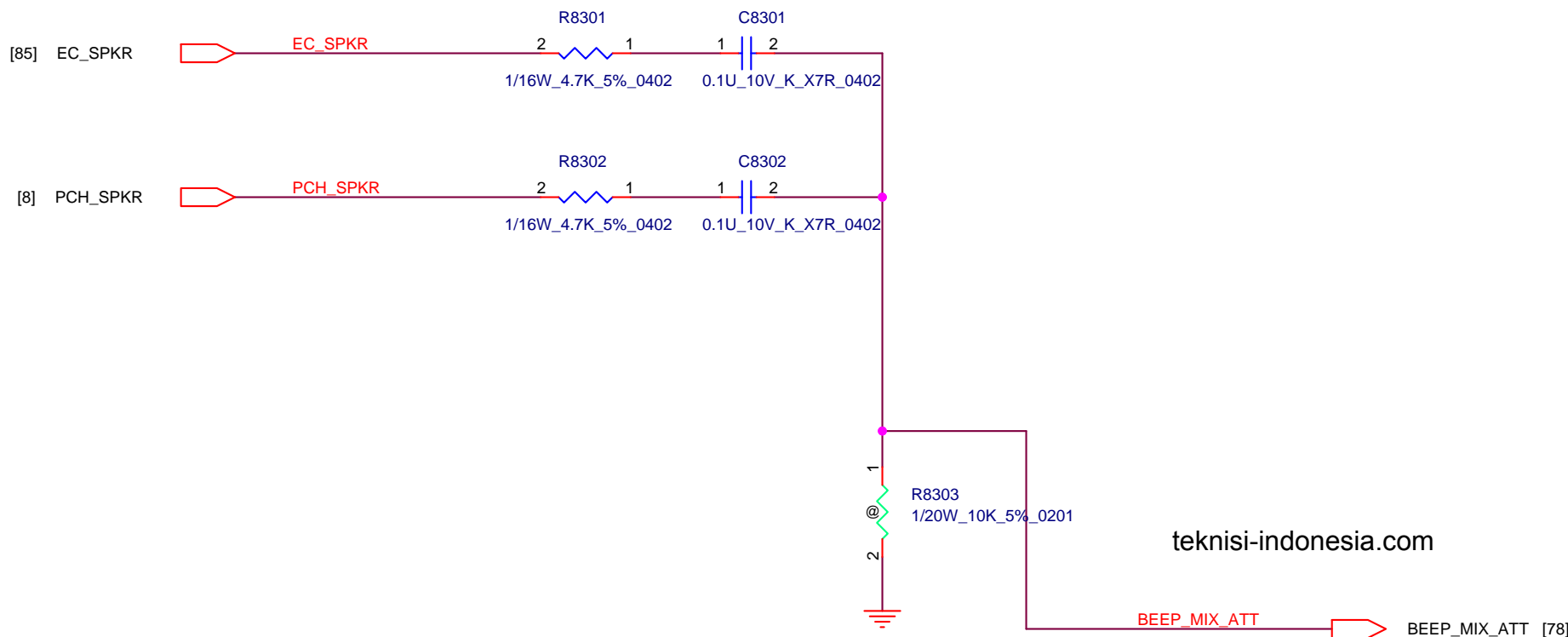
NEAR EXT MIC CONN

SPK CONN.



Security Classification	LC Future Center Secret Data			Title	AUDIO JACK SENSE	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	Size	Custom	Document Number
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Audio BEEP



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Title			
AUDIO BEEP			
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FUNCTION TABLE

A _{SEL}	V _{AUDIO}	V _{BUS}	L,R	D+, D-
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF ⁽¹⁾	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.

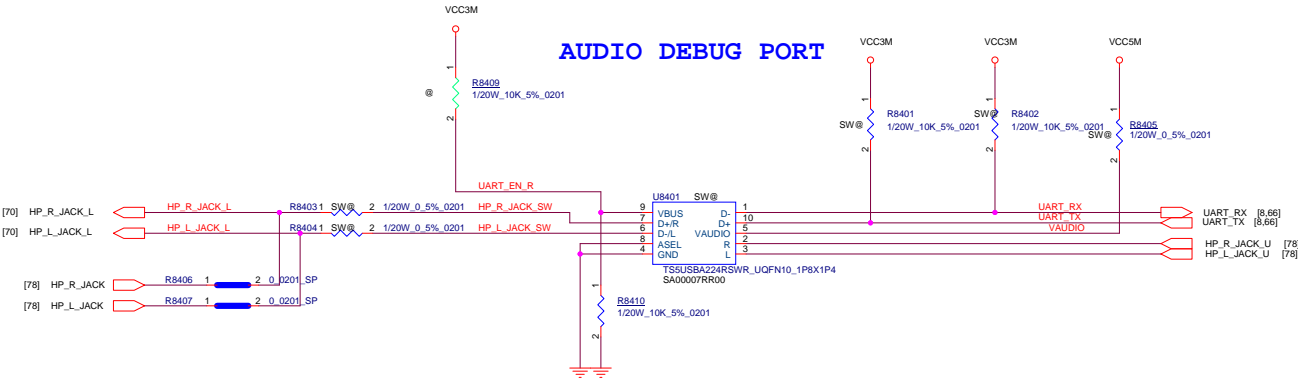
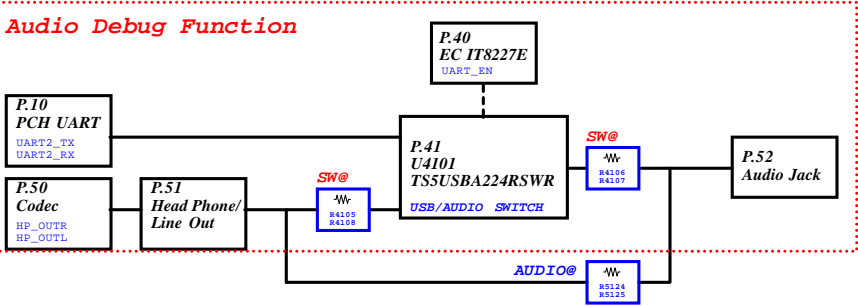
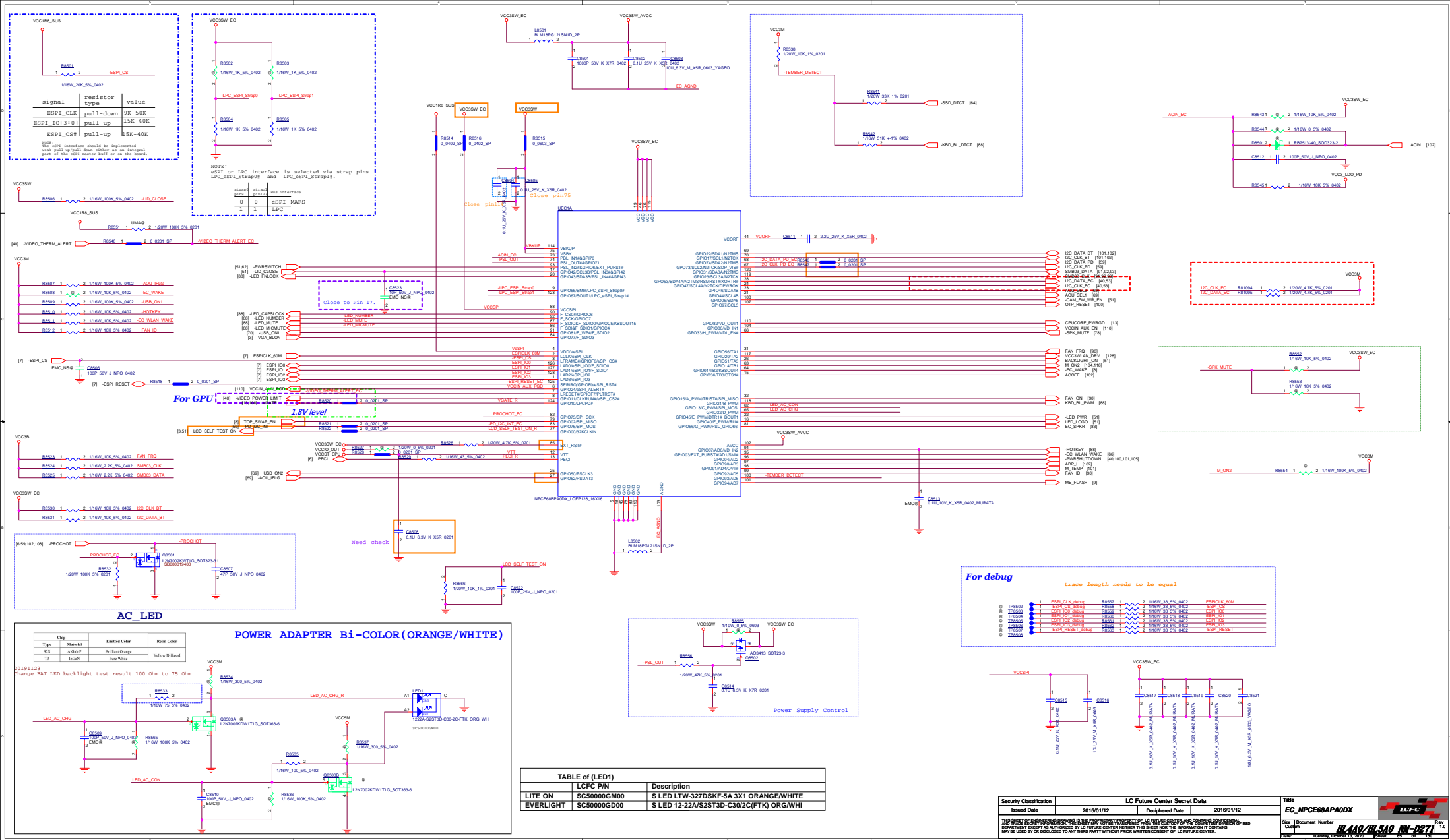


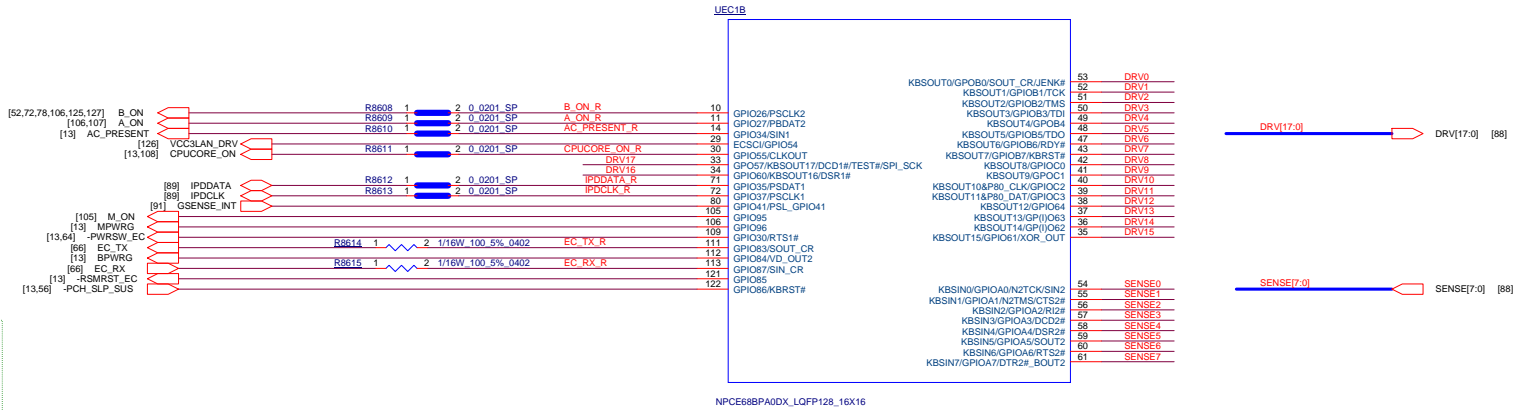
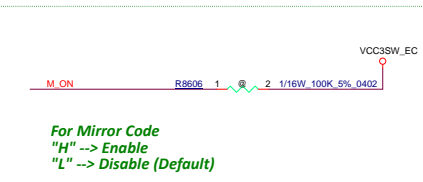
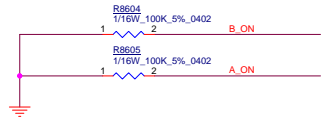
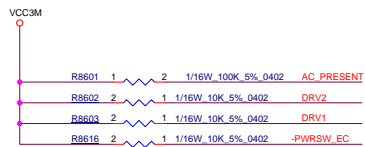
TABLE:

Mode	Audio	UART
UART_EN	L	H


TABLE:

Part Name	For NPI	For MP
U8401 SW@	ASM	NA
R8403 SW@	ASM	NA
R8404 SW@	ASM	NA
R8401 SW@	ASM	NA
R8402 SW@	ASM	NA
R8405 SW@	ASM	NA
R8506 AUDIO@	NA	ASM
R8507 AUDIO@	NA	ASM

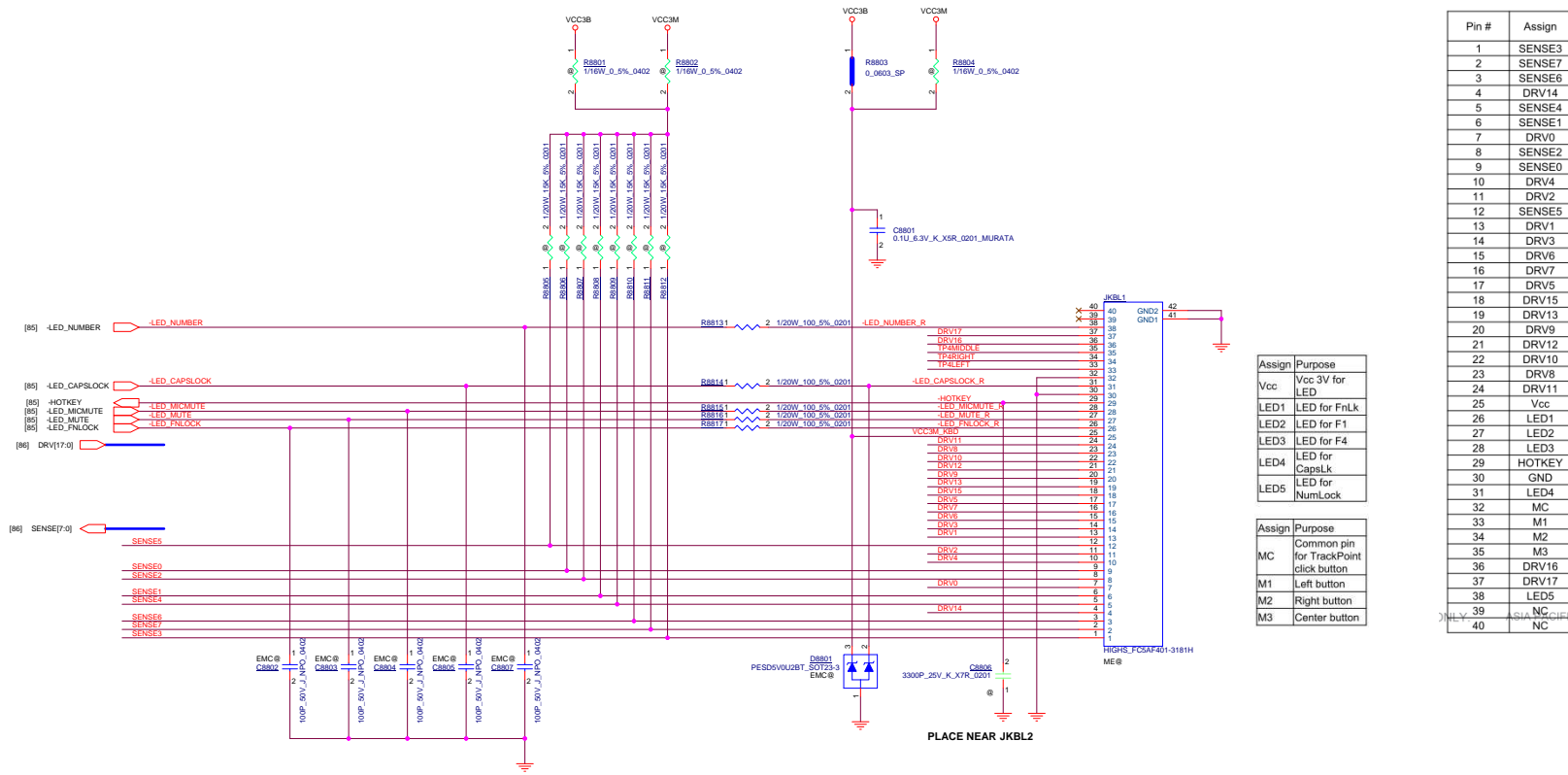




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				<div></div> <div>Rev 1.0</div> <div>Sheet 87 of 130</div>	

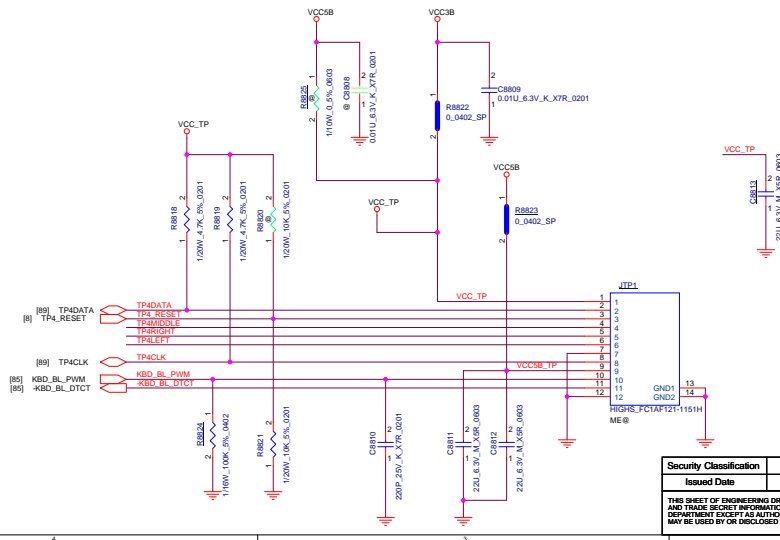
Keyboard CONN



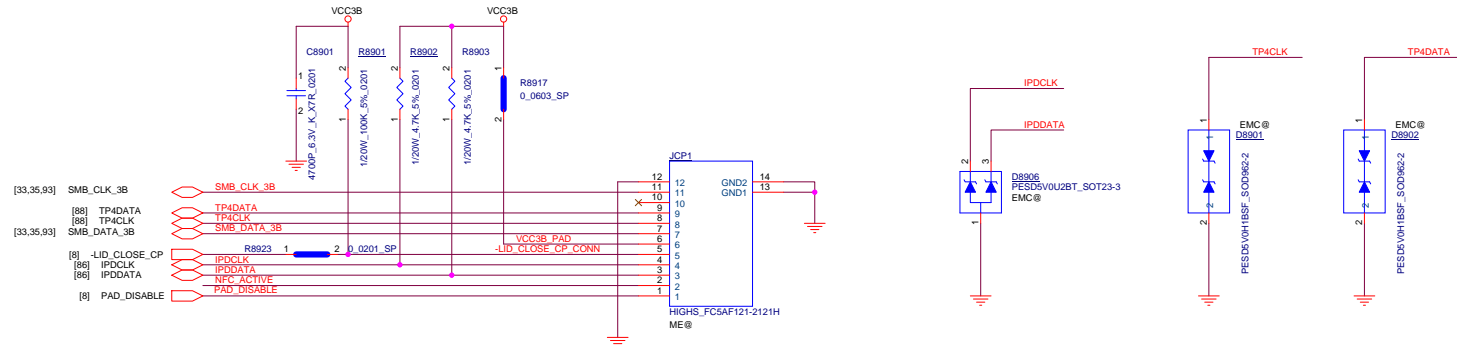
Track Point

TrackPoint and Backlight FPC Pin Assignment

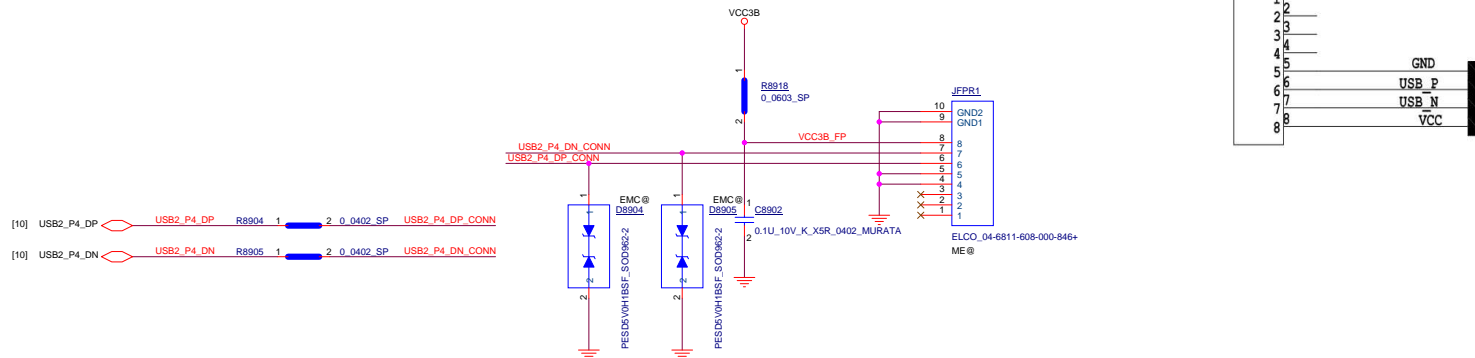
Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND



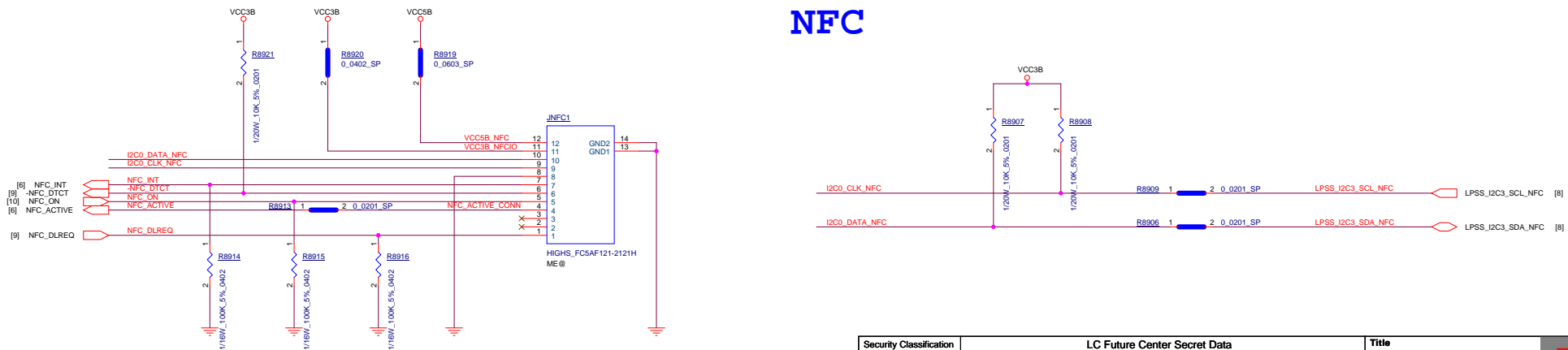
Click Pad



FingerPrint Conn

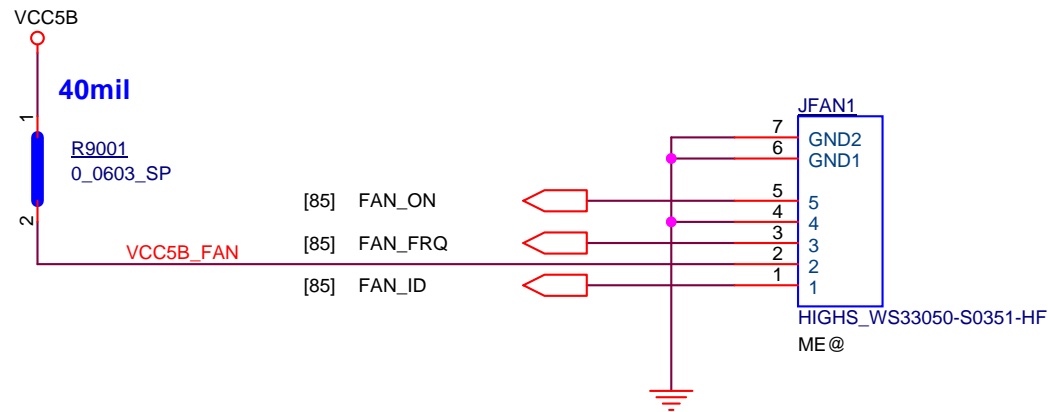


NFC



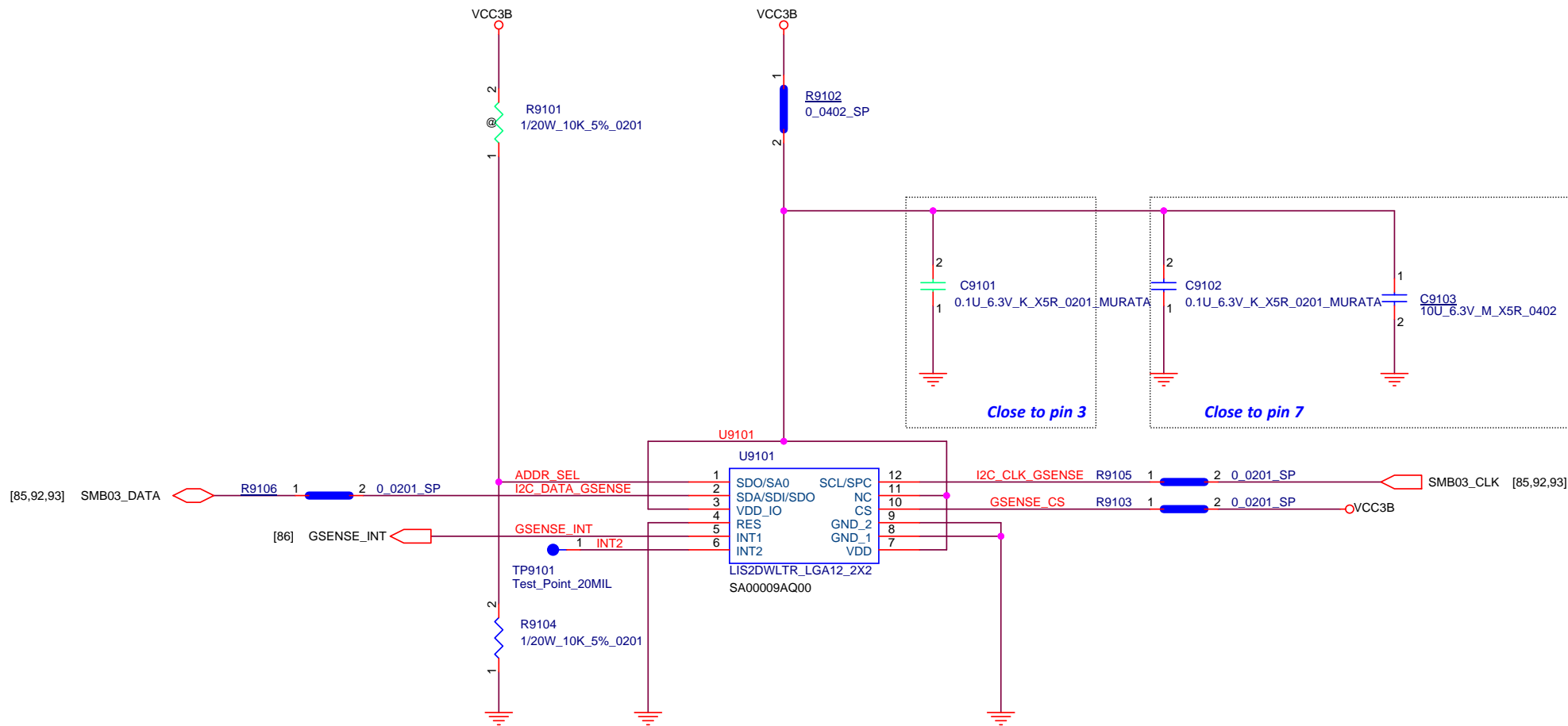
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	TOUCH PAD/NFC/FPR	
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FAN CONN.



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Title			
FAN CONNECTOR			
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Custom	HL4A0/HL5A0 NM-D271	1.0	
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TABLE

TABLE of G-Sensor (U9101)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA280	SA0000A1600

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BMA280	H	0011001b(0x19)
	L	0011000b(0x18)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

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Issued Date	2015/01/12	Deciphered Date	2016/01/12	APS G-SENSOR	
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				Rev 1.0	

Thermal Sensor Close to DIMM

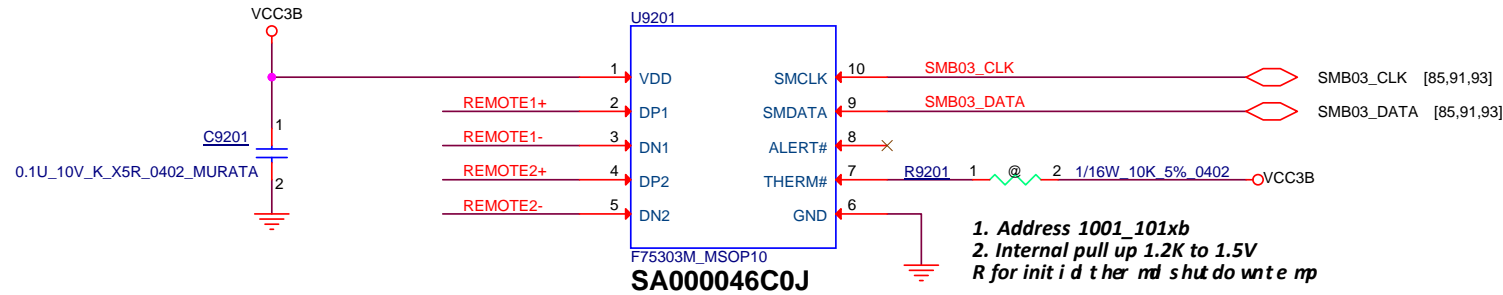
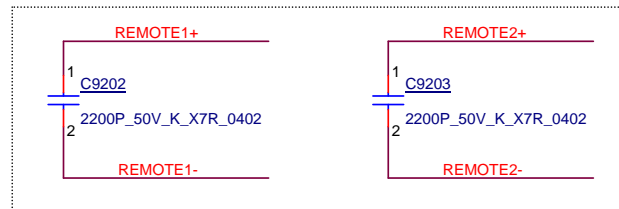
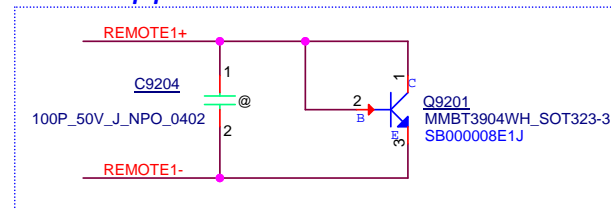


TABLE of Thermal Sensor (U9201)

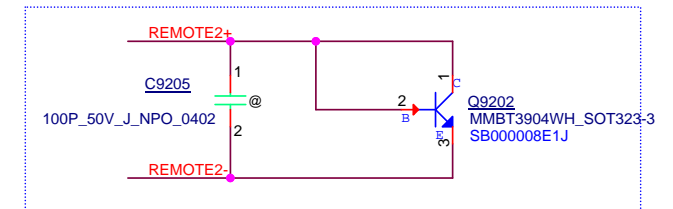
Vendor	LCFC P/N	Description
FINTEK	SA000046C0J	S IC F75303M MSOP 10P SENSOR
Nuvoton	SA000065D00	S IC NCT7719W MSOP 10P THERMAL SENSOR



Under the pipe




Close to SSD



*Trace width/space:10/10 mil
Trace length:<8"*

TABLE of Thermal Sensor (Q9201,Q9202)

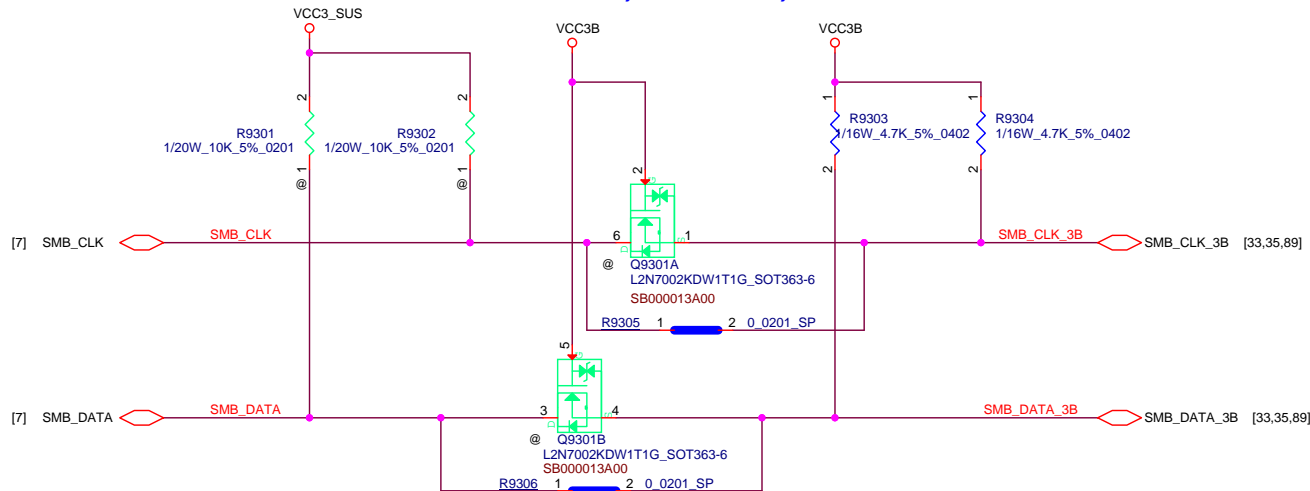
Vendor	LCFC P/N	Description
PANJIT	SB000008E1J	S TR MMBT3904WH NPN SOT323-3
LRC	SB00000ZJ00	S TR LMBS3904WT1G NPN SOT323-3
NXP	SB00000YV00	S TR PMST3904 NPN SOT323-3

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Issued Date	2015/01/12	Deciphered Date	2016/01/12	THERMAL SENSOR		
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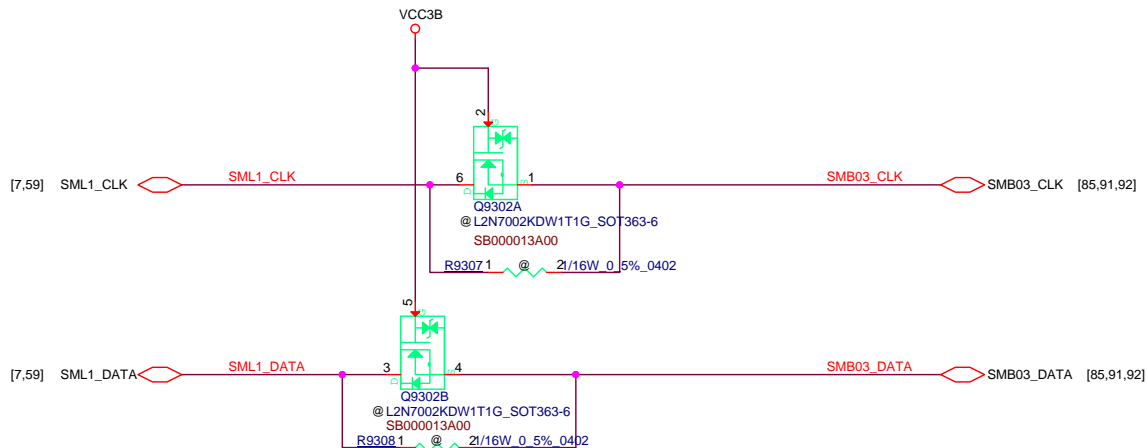
HL4A0/HL5A0 NM-D271

SMBus

DIMM1,DIMM2,CP



GPU, Thermal Sendor,
Embedded Controller, G sensor



2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV

TABLE of U9301/U9302/U9303/U9304


Vendor	P/N	LCFC P/N
TI	SN74LVC1G66DCK	SA00005BE0J
NXP	74LVC1G66GW	SA00007KS00
ONsemi	MC74VHC1G66DFT2G	SA00008JQ00

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				C	HL4A0/HL5A0 NM-D27I	1.0
				Date:	Tuesday, October 13, 2020	Sheet 95 of 130

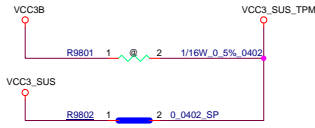
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	SATA HDD CONN	
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				Sheet 96 of 130	

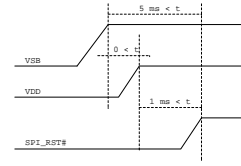


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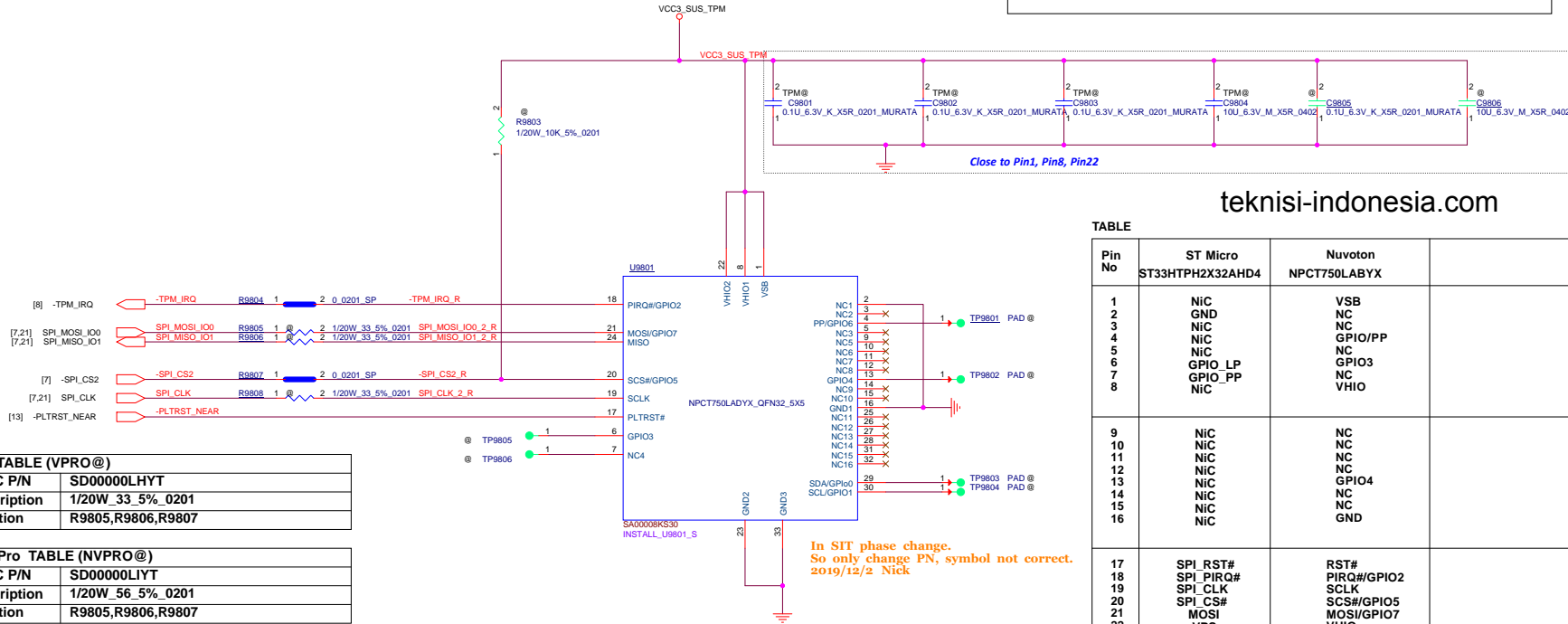
Security Classification		LC Future Center Secret Data		Title		
Issued Date		2015/01/12	Deciphered Date	2016/01/12	SATA RE-DRIVER	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>						
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NOTE:
Check timing sequence in SDV phase.



- NOTE:
- 1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
 - 2) SPI_RST# must be asserted for at least 5 msec after VSB power-up.
 - 3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
 - 4) SPI_RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5v above the VDD power level.



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TABLE

Pin No	ST Micro ST33HTPH2X32AHD4	Nuvoton NPCT750LABYX	
1	NIC	VSB	
2	GND	NC	
3	NIC	NC	
4	NIC	GPIO/PP	
5	NIC	NC	
6	GPIO_LP	GPIO3	
7	GPIO_PP	NC	
8	NIC	VHIO	
9	NiC	NC	
10	NiC	NC	
11	NiC	NC	
12	NiC	NC	
13	NiC	GPIO4	
14	NiC	NC	
15	NiC	NC	
16	NiC	GND	
17	SPI_RST#	RST#	
18	SPI_PIRQ#	PIRQ#/GPIO2	
19	SPI_CLK	SCLK	
20	SPI_CS#	SCS#/GPIO5	
21	MOSI	MOSI/GPIO7	
22	VPS	VHIO/GPIO7	
23	NiC	GND	
24	MISO	MISO	
25	NiC	NC	
26	NiC	NC	
27	NiC	NC	
28	NiC	NC	
29	NiC	SDA/GPIO0	
30	NiC	SDA/GPIO0	
31	NiC	NC	
32	NiC	NC	

vPro TABLE (VPRO@)	
LCFC P/N	SD00000LHYT
Description	1/20W_33_5%_0201
Location	R9805,R9806,R9807

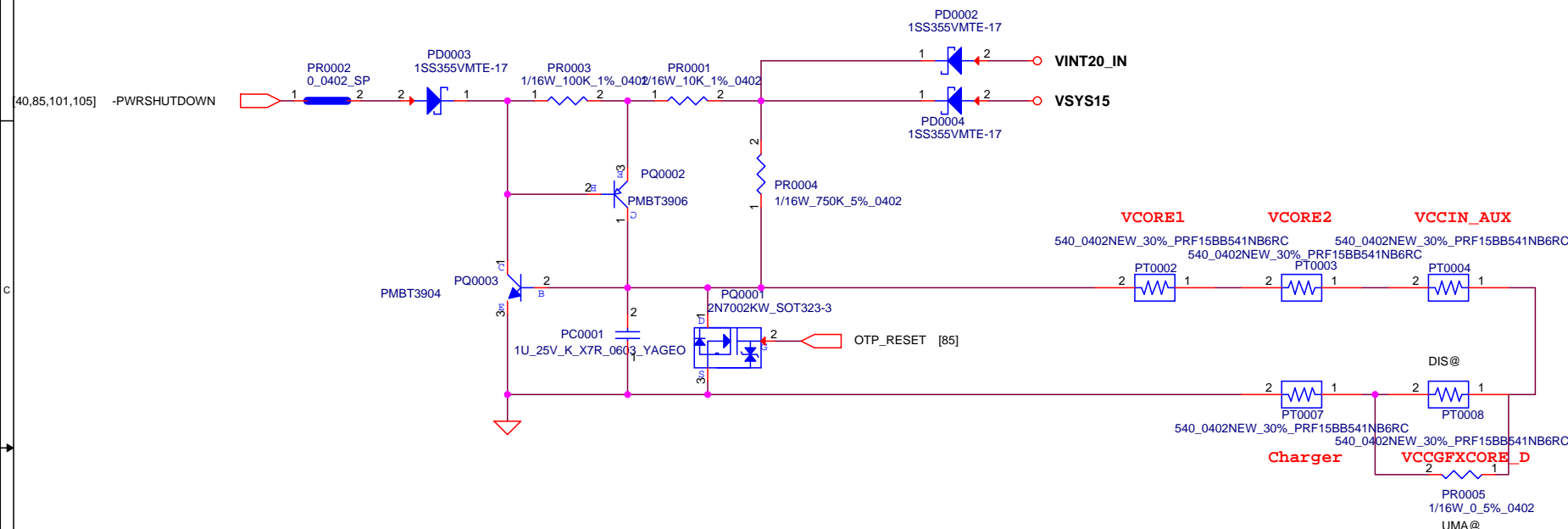
Non-vPro TABLE (NVPRO@)	
LCFC P/N	SD00000LIYT
Description	1/20W_56_5%_0201
Location	R9805,R9806,R9807


TABLE of TPM (U9801)		
Vendor	LCFC P/N	Description
NUVOTON	SA00008KS30	S IC NPCT750LADYX QFN 32P TPM 2.0
ST	SA0000AB720	S IC ST33HTPH2X32AHD8 VQFN 32P TPM 2.0

For ME GND hole Screw Hole

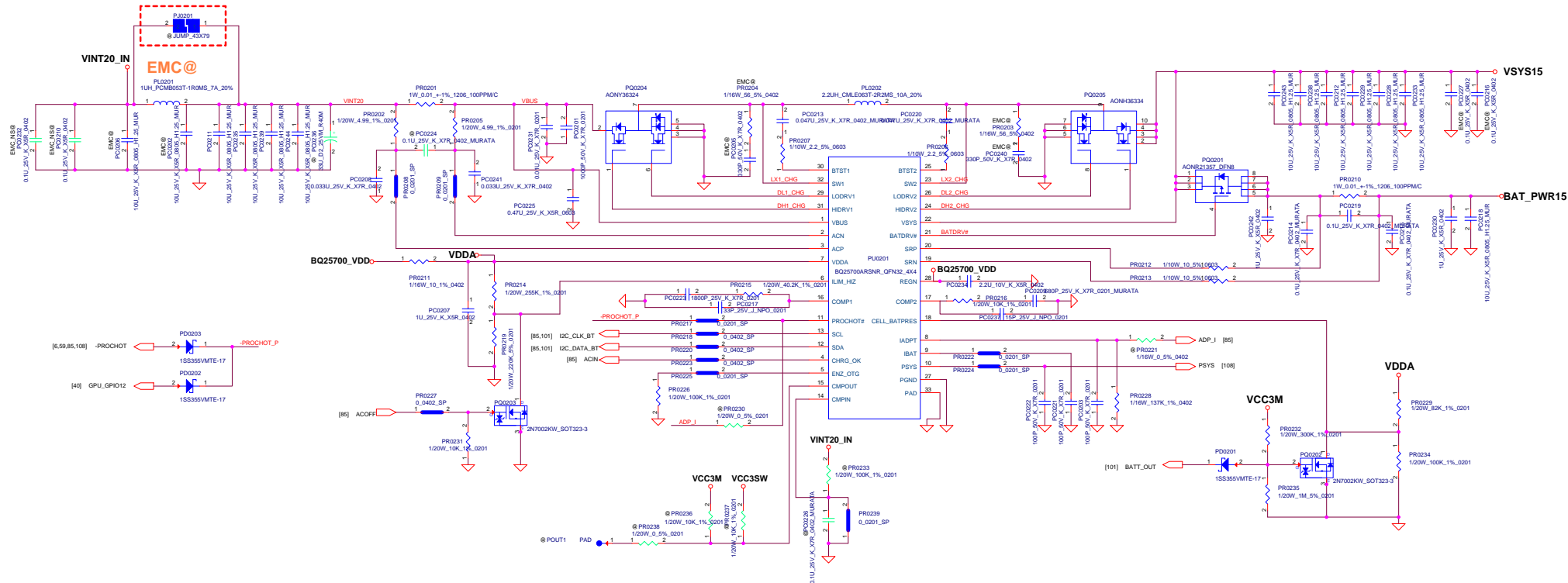


VINT20_IN [59,60,102]
 VSYS15 [51,102,103,104,105,106,108,109,110,117,118]
 VCC3SW [20,51,85,101,102,105,126,127]
 RTCVCC [13,16,20]



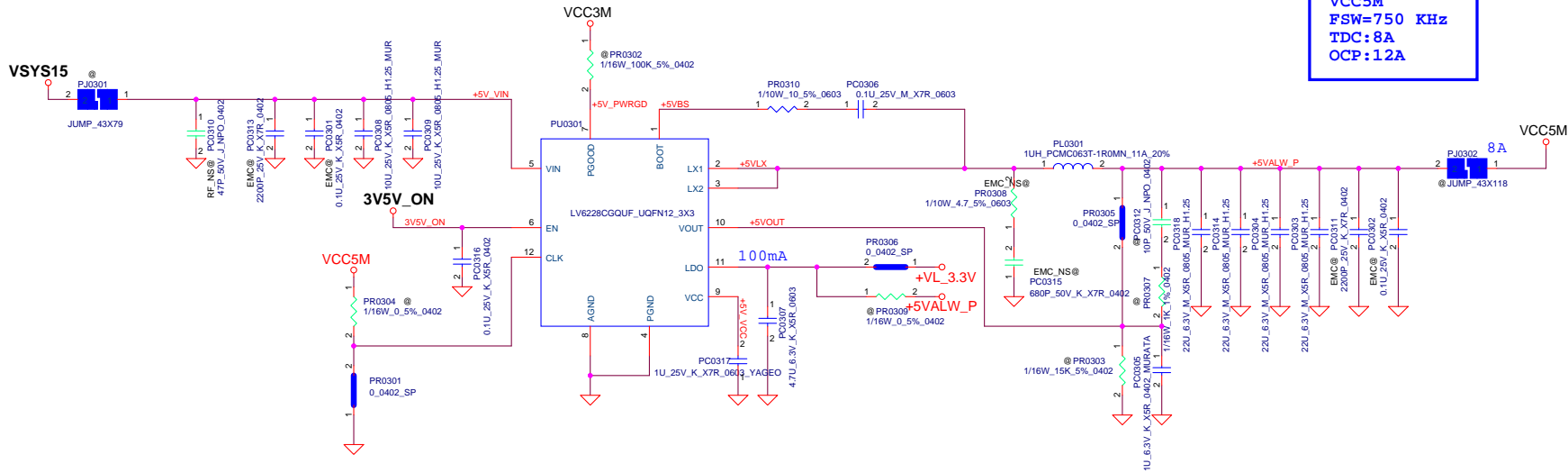
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VINT20_IN [59,60,100]
VSY515 [51,100,103,104,106,108,109,110,117,118]
BAT_PWR15 [101]



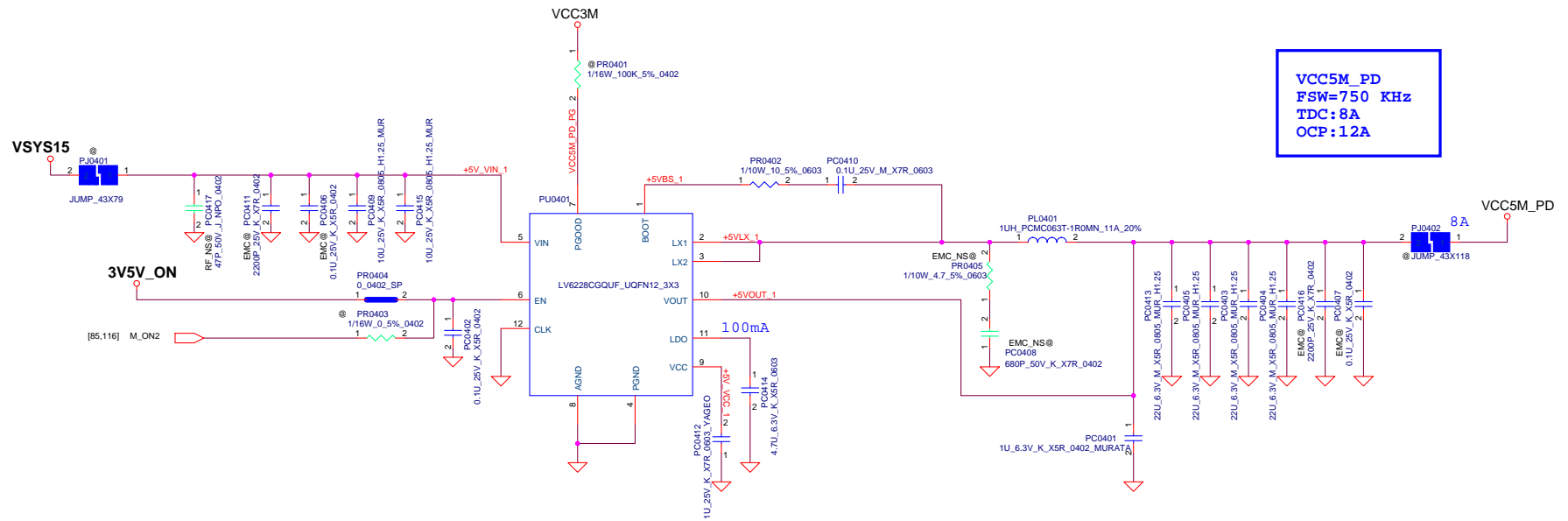
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Issued Date		Deciphered Date		BATTERY CHARGER(BQ25700A)	
2013/08/05		2014/12/31			
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		128			

VSYS15 [51,100,102,104,105,106,108,109,110,117,118]
VCC5M [51,69,70,72,84,85,107,108,109,110,116,117,118,119,120,125,126,127]



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Issued Date		Deciphered Date		DC/DC VCC5M (LV6228)		
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				Date:	Tuesday, October 13, 2020	Sheet 103 of 128

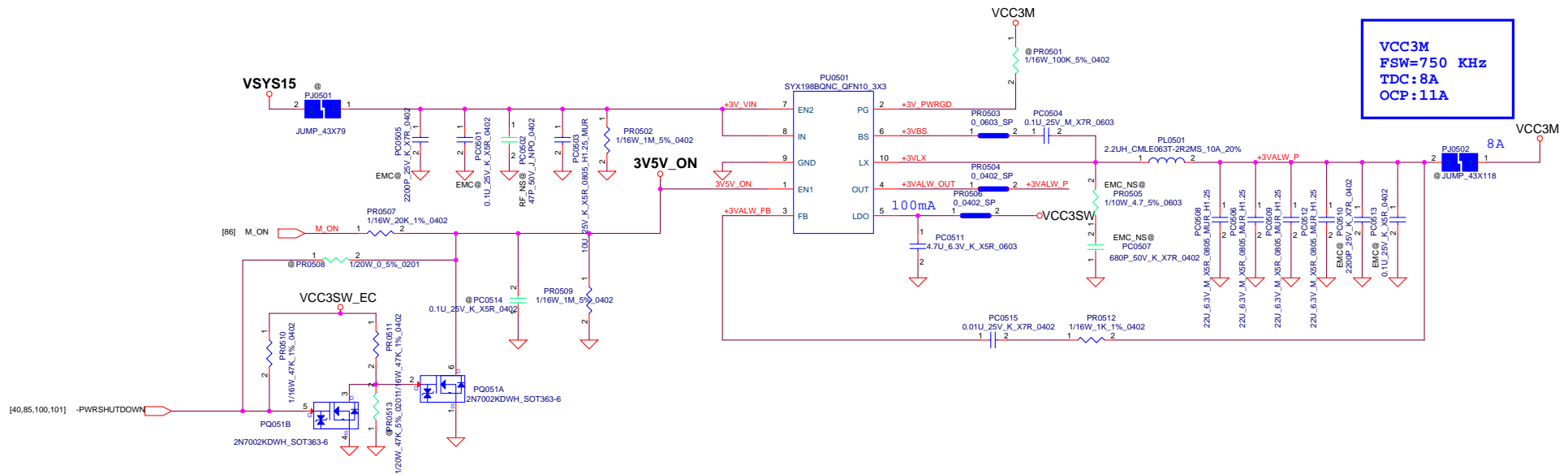
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VCC5M_PD [59]




VCC5M_PD
FSW=750 KHz
TDC:8A
OCP:1.2A

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			Rev 2.0
			Date: Tuesday, October 13, 2020 [Sheet 104 of 128]

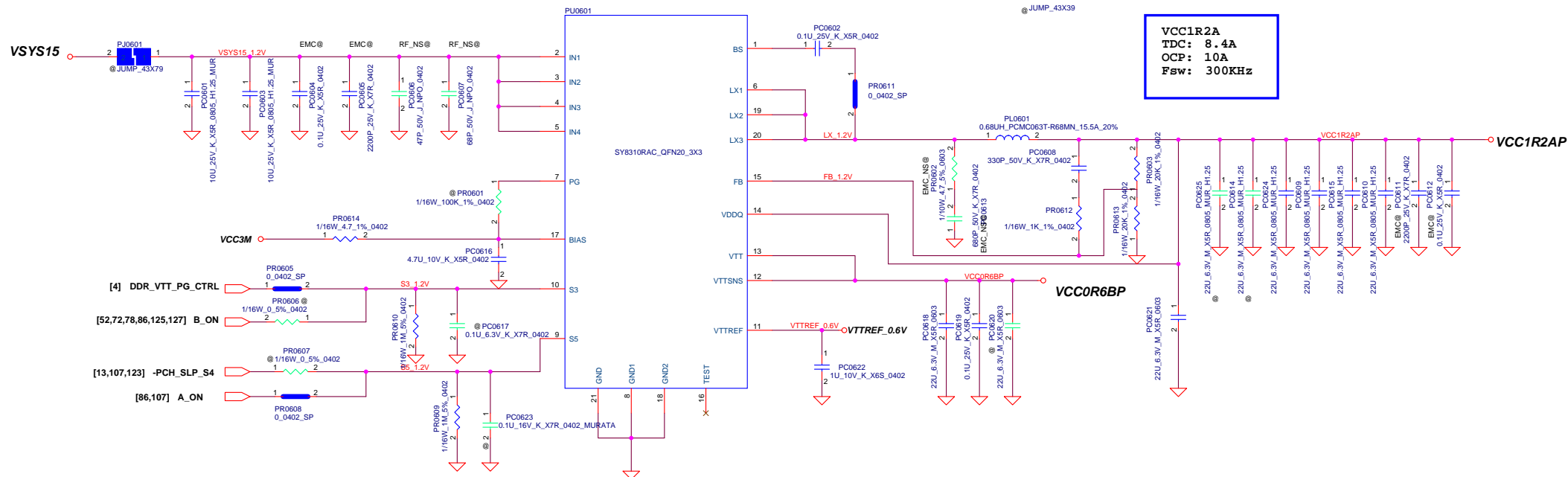
VSYS15 [51,100,102,103,104,106,108,109,110,117,118]
VCC3M [4,13,16,51,52,55,56,59,84,85,86,88,102,103,104,106,110,116,118,119,120,123,124,125,126,127,128]




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				Document Number GL4A0/GL5A0 NM-C632
				Rev 2.0
				Date: Tuesday, October 13, 2020 Sheet 105 of 128

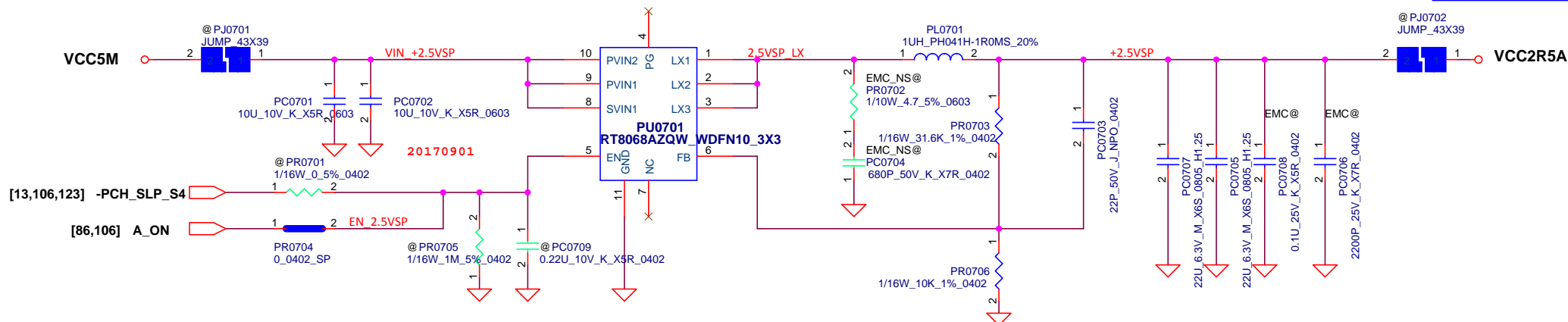
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VCC1R2A [4,5,14,15,33,34,35,36]
VCC0R6B [33,34,35,36]



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Issued Date	2013/08/05	Deciphered Date	2014/12/31	DC/DC VCC1R2A(RT8231)	
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VCC5M VCC5M [51,69,70,72,84,85,103,108,109,110,116,117,118,119,120,125,126,127]
VCC2R5A VCC2R5A [33,34,35,36]

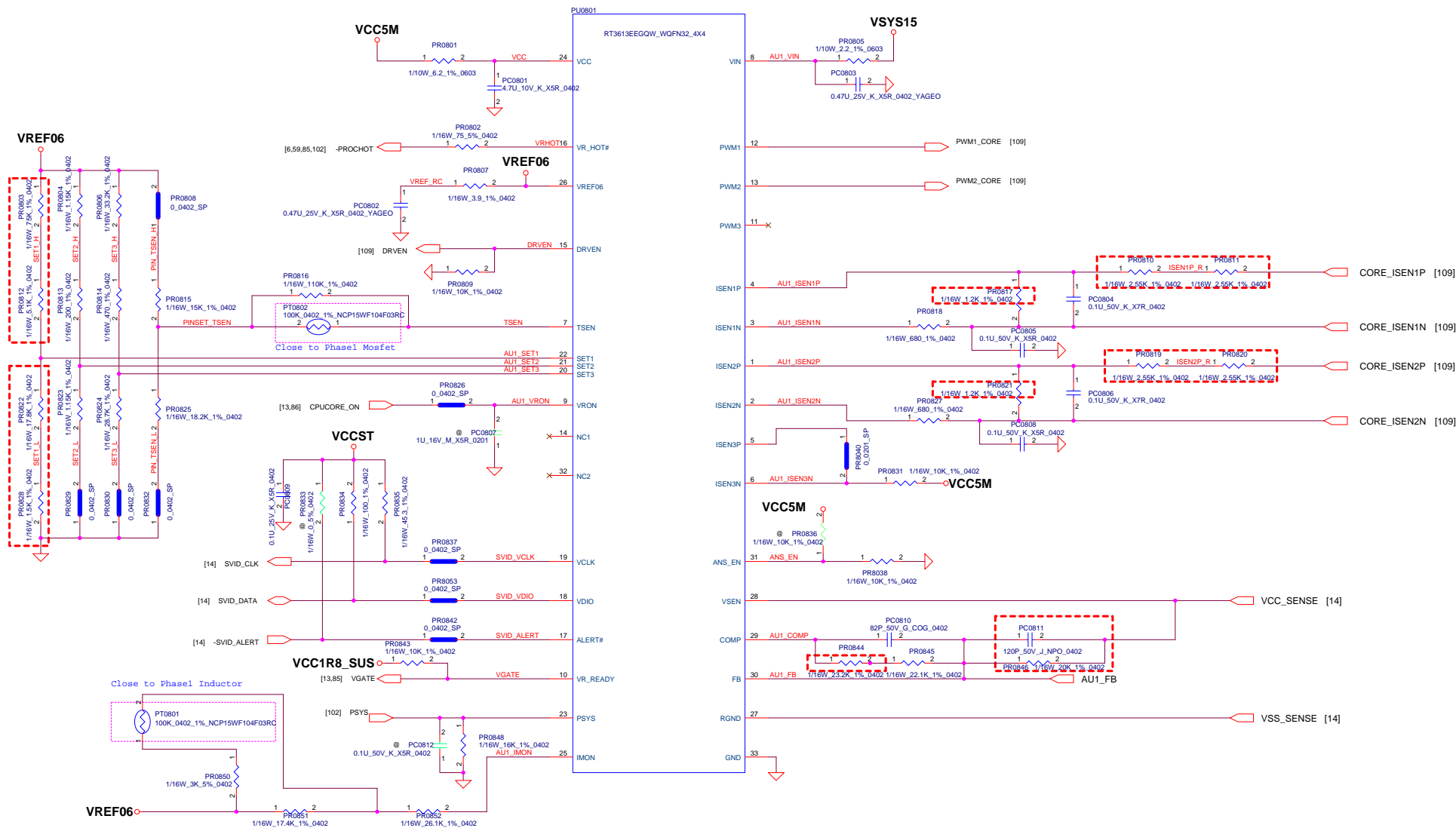
VCC2R5A
TDC: 2A
OCP: 4A
Fsw: 1MHz

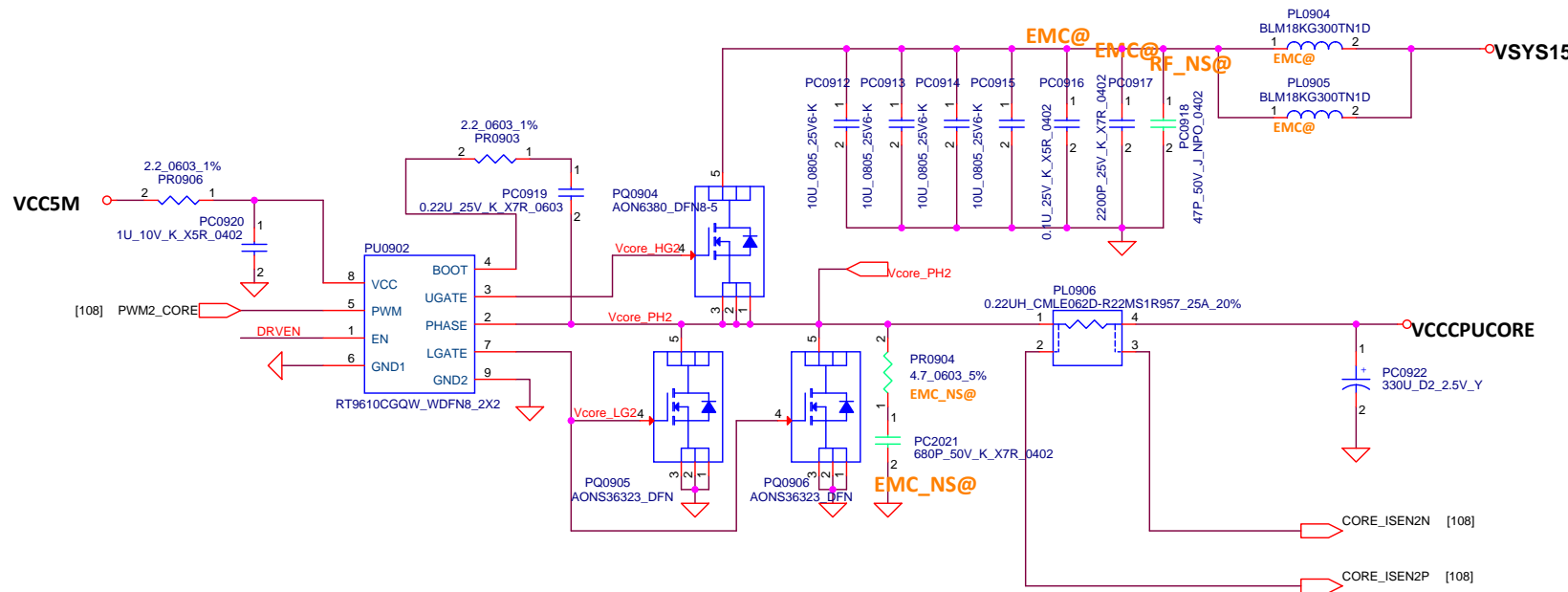
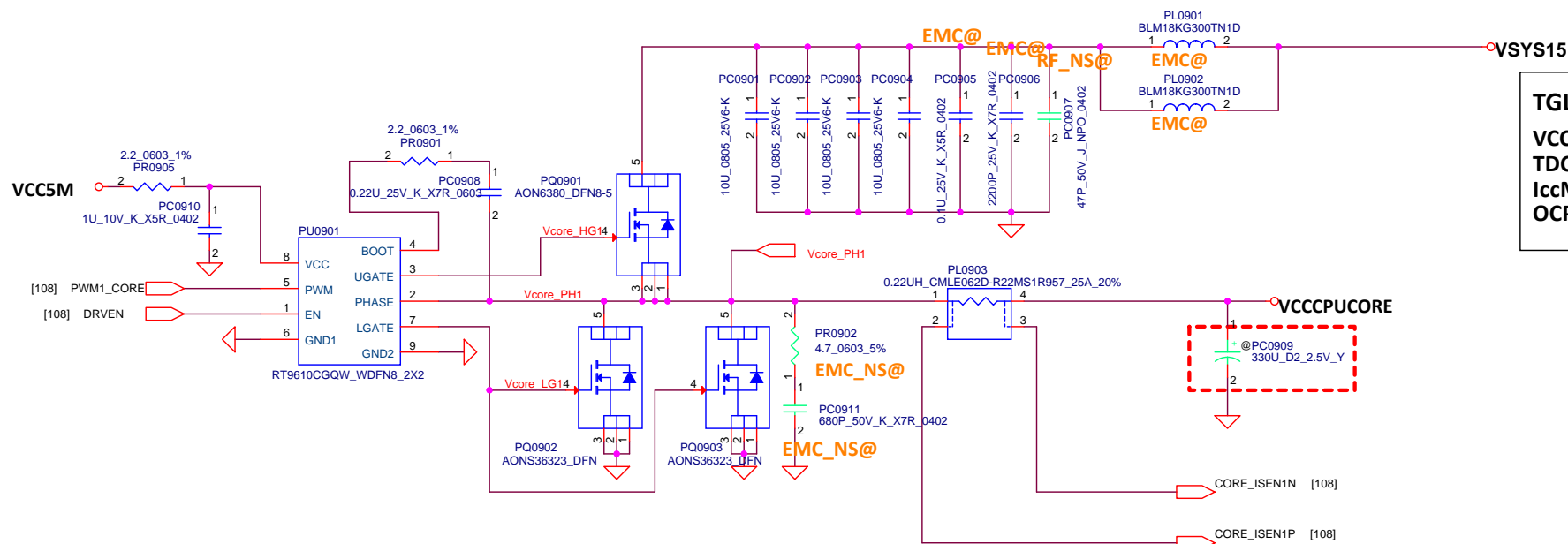


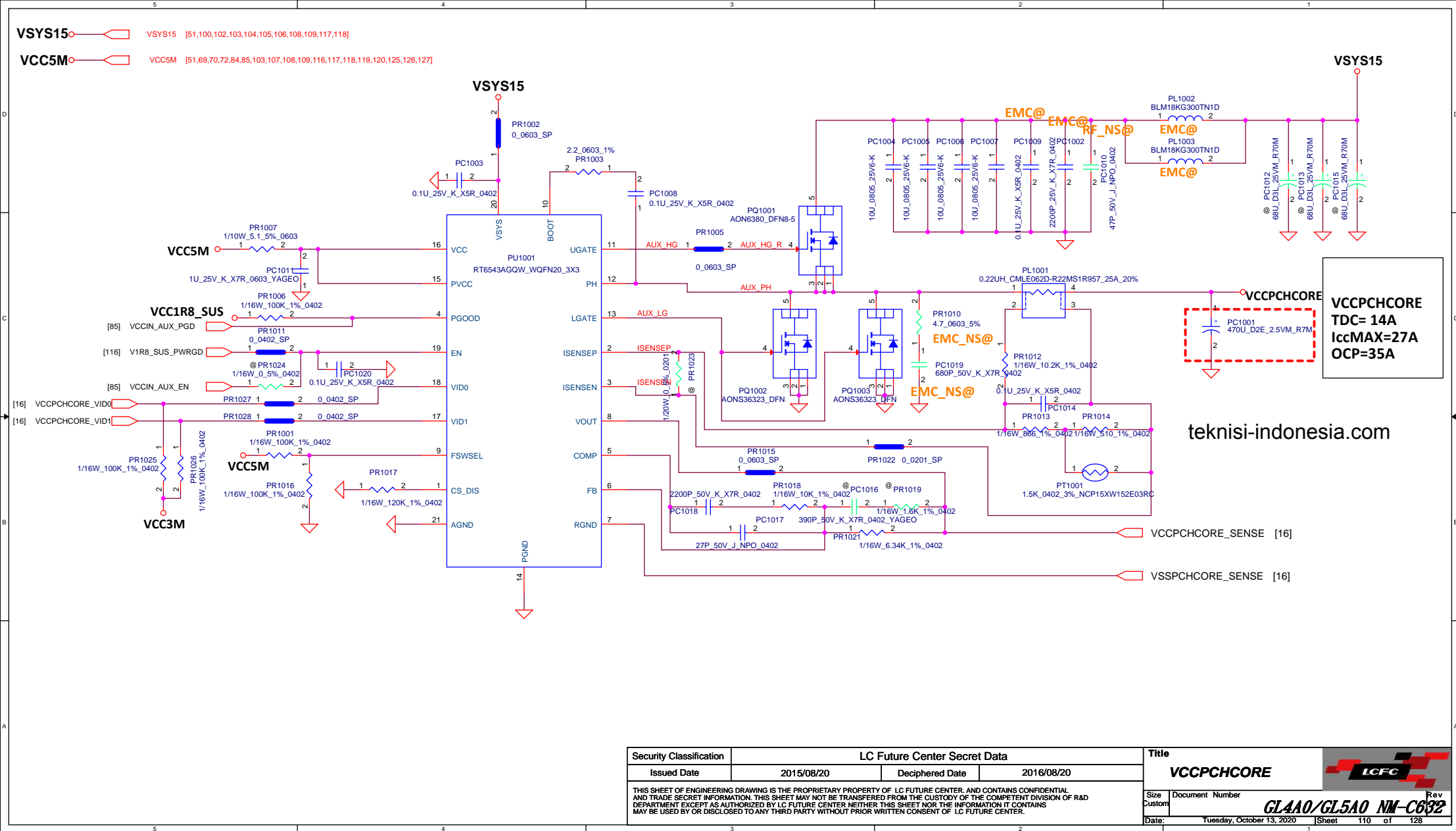
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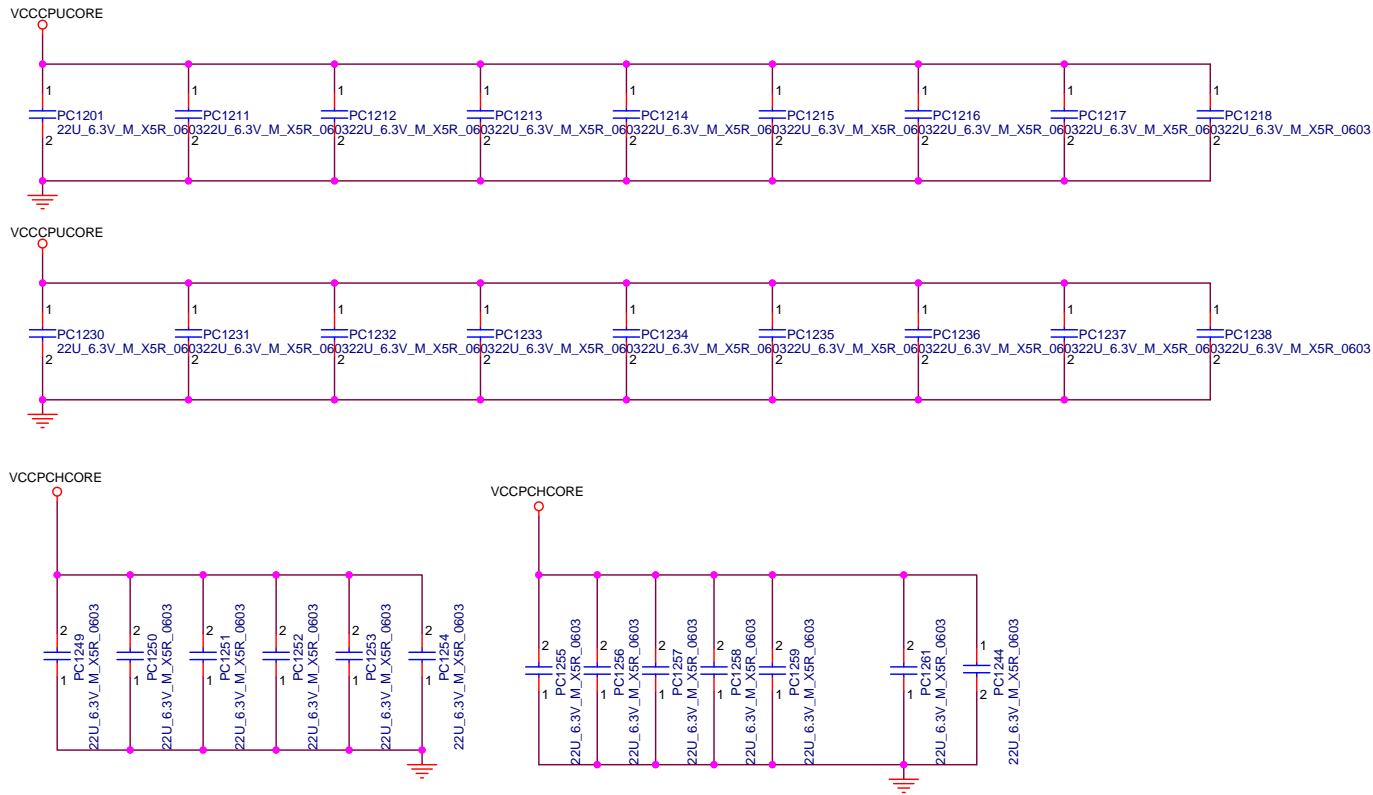






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				Sheet		113 of 128


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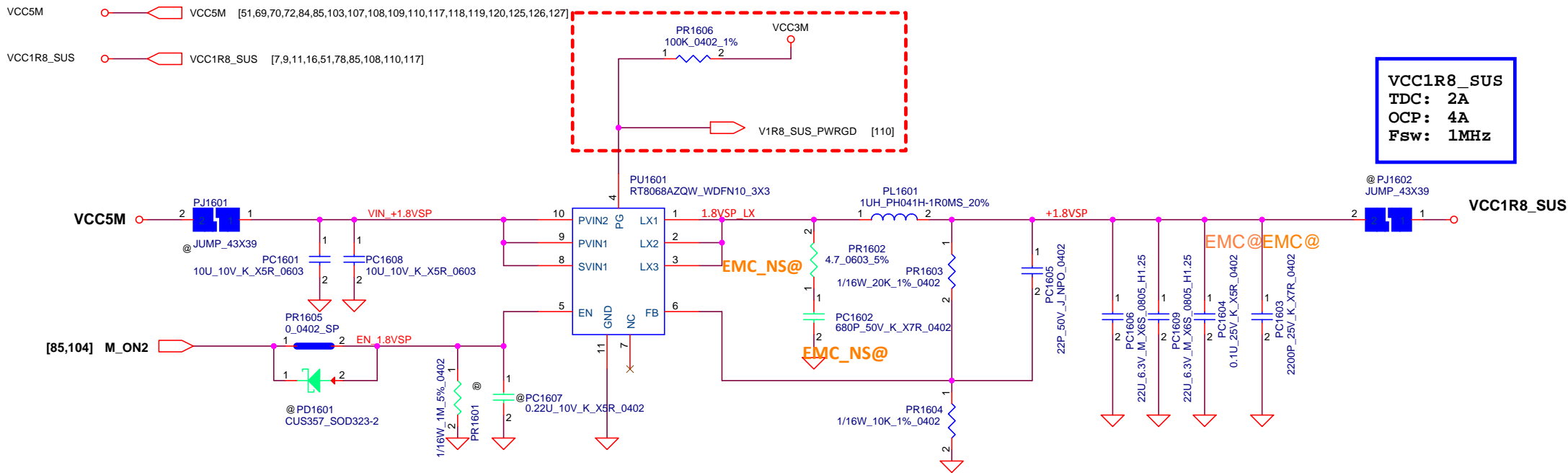
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Rev

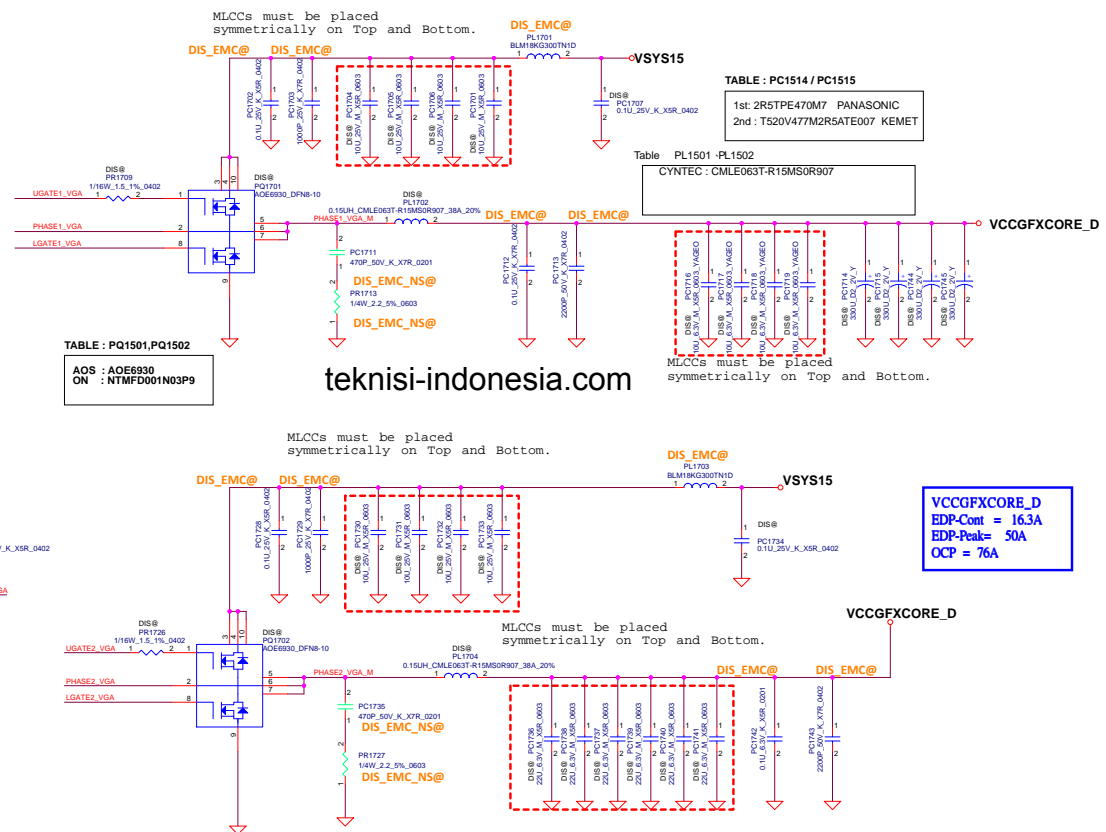
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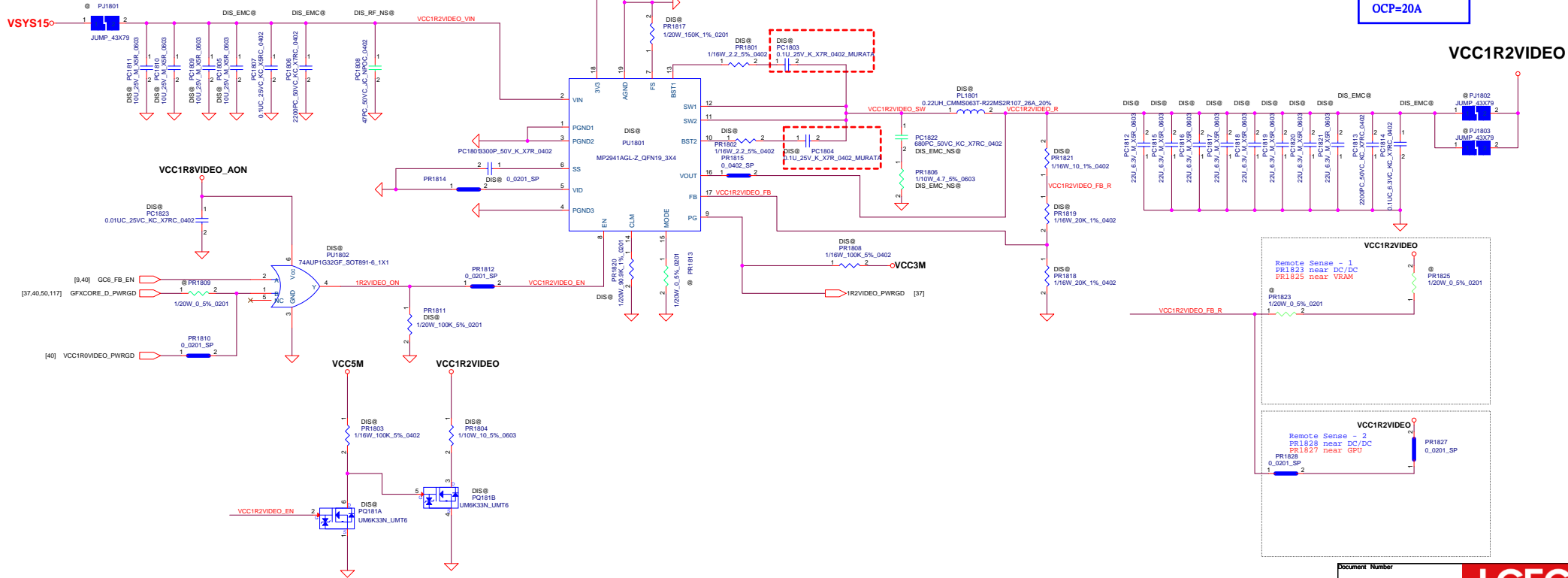
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				<div><div></div><div>Rev 0.1</div></div>	
				Sheet 115 of 128	




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Date: Tuesday, October 13, 2020				Sheet	122	of 130

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VCC3M

VCC3_SUS

R12401 1 2 0_0805_SP

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1.0

Date:

Tuesday, October 13, 2020

Sheet

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Pin 15: VCC3B_SSD



TABLE of POWER SWITCH (U12501)		
Vendor	LCFC P/N	Description
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
DII	SA000075900	S IC AP22966DC8-7 V-DFN3020 14P LOAD SWI

Vendor	LCFC P/N	Description
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
DII	SA000075900	S IC AP22966DC8-7 V-DFN3020 14P LOAD SWI



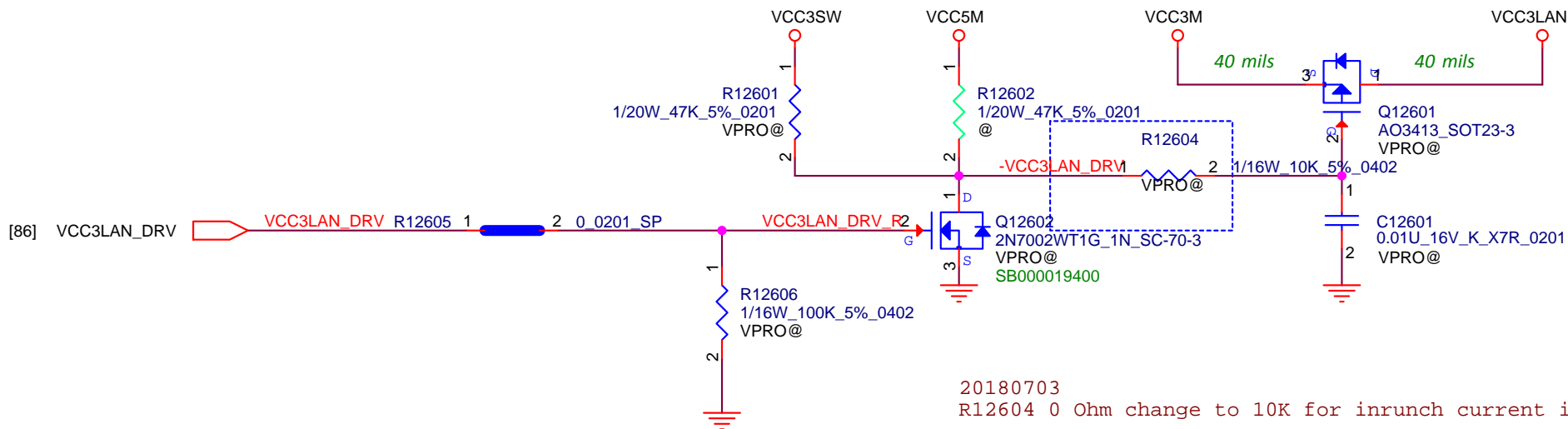
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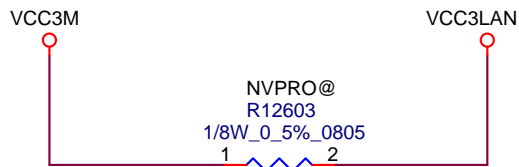
VCC3LAN VCC3LAN [62,73]


Due to solve G3 to S5 wake on lan issue
+3VALW must meet INTEL spec.
Control LAN power sequence must be stuff.

For VPRO

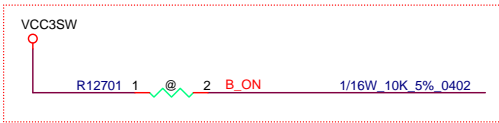


For NVPRO

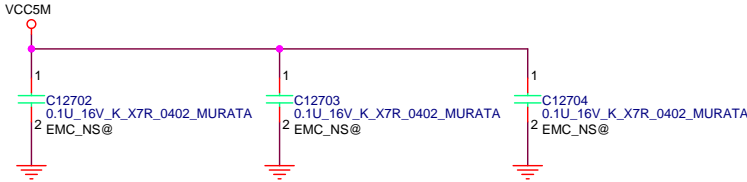


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Date:		Tuesday, October 13, 2020				Sheet		126 of 130			

VCC3SW		VCC3SW	[20,51,85,101,102,105,126]
VCC3M		VCC3M	[4,13,16,51,52,55,56,59,84,85,86,88,102,103,104,105,106,110,116,118,119,120,123,124,125,126,128]
VCC5M		VCC5M	[51,69,70,72,84,85,103,107,108,109,110,116,117,118,119,120,125,126]
VCC5B		VCC5B	[54,72,78,88,89,90]
VCC3B		VCC3B	[3,7,8,10,12,13,33,34,35,36,37,51,52,53,55,57,58,63,64,66,67,70,73,76,78,85,88,89,91,92,93,98,101]



1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.



Smart Switch

VCC5M To VCC5B

VCC3M To VCC3B

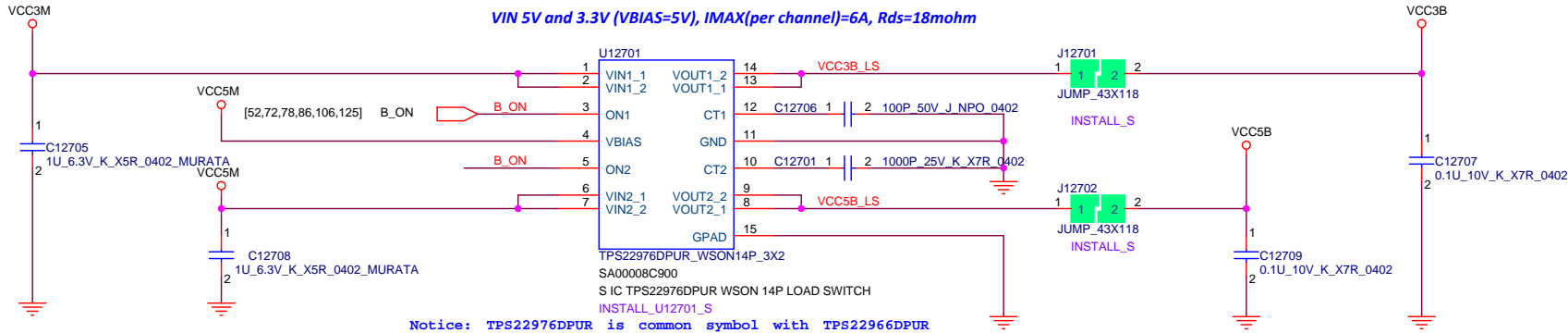


TABLE of POWER SWITCH (U12701)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH
RICHTEK	SA000067200	S IC RT9740AGQW WDFN 14P LOAD SWITCH

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				Date:	Tuesday, October 13, 2020	Sheet 127 of 130

VCC3WLAN VCC3WLAN [8,9,66]

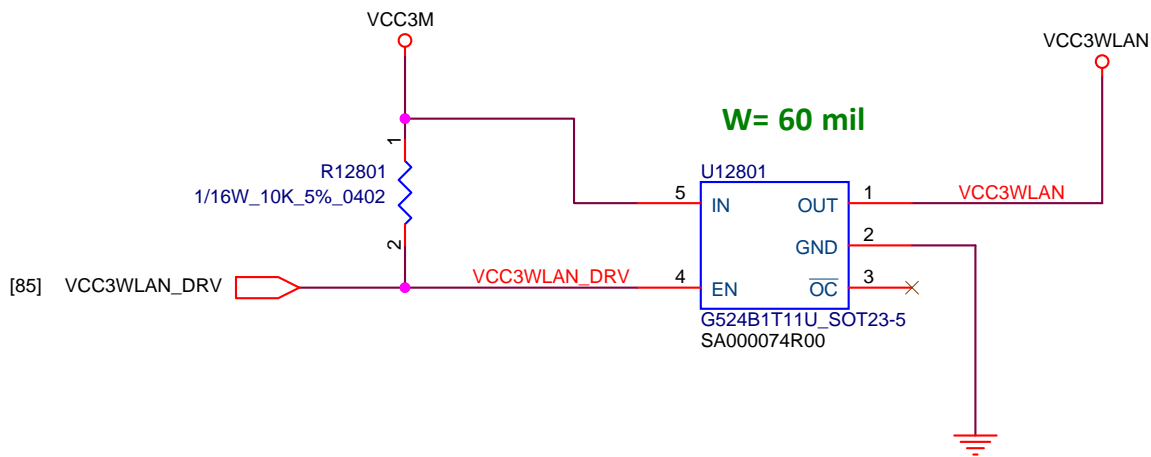
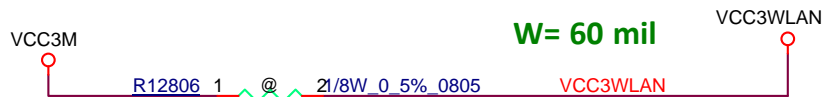


TABLE of POWER SWITCH (U12801)

Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
RICHTEK	SA0000AGK00	S IC RT9742NGJ5 TSOT-23-5 5P PWR SW
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

Security Classification

LC Future Center Secret Data

Title

LOAD SW WLAN



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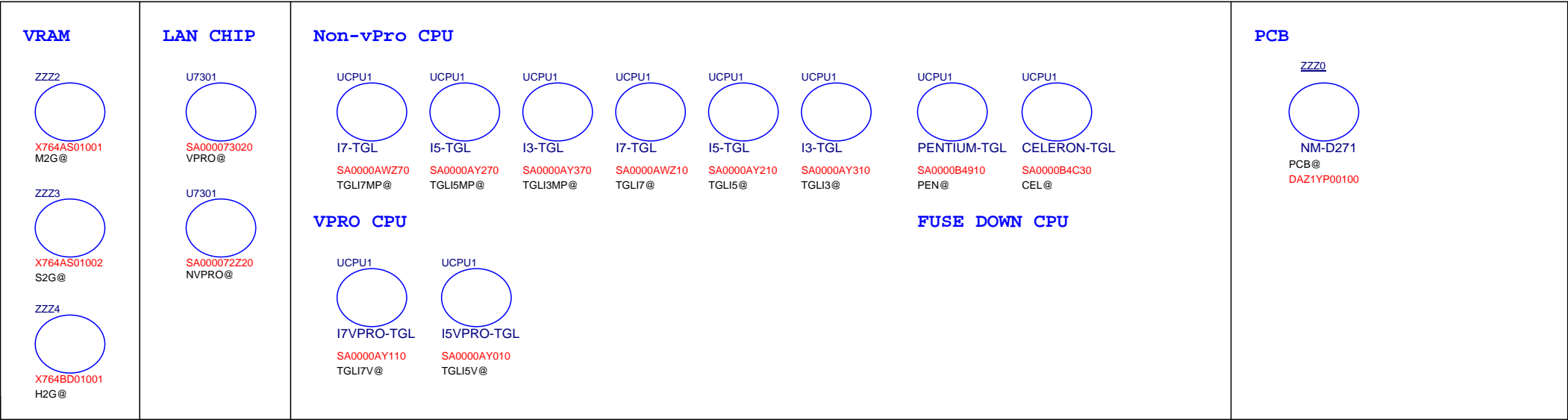
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Power On Sequence - Non Deep Sx

